

# 1. Schematic Page Description :

## ZRU/Vichy Schematic Ver : 1.0

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- |                                 |                                  |
|---------------------------------|----------------------------------|
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| 02 -- Block Diagram             | 22 -- TPM                        |
| 03 -- Valley 1/9 (DDRA)         | 23 -- DB /Thermal sensor/LID     |
| 04 -- Valley 2/9 (DDRb)         | 24 -- Audio Codec/SPK/DMIC       |
| 05 -- Valley 3/9 (Display)      | 25 -- Audio Headset Switch/HP    |
| 06 -- Valley 4/9 (SD/PCIE/SATA) | 26 -- USB3/Hole                  |
| 07 -- Valley 5/9 (SPI/GPIO/CLK) | 27 -- KB/TP/HW RST               |
| 08 -- Valley 6/9 (USB/LPC/I2C)  | 28 -- KBC                        |
| 09 -- Valley 7/9 (Power 1)      | 29 -- Charger (BQ24717RGRR)      |
| 10 -- Valley 8/9 (Power 2)      | 30 -- SYSTEM 5V/3V (TPS51225BR)  |
| 11 -- Valley 9/9 (GND)          | 31 -- Load Switch                |
| 12 -- BTM XDP & APS             | 32 -- DDR 1.35V(TPS51216)        |
| 13 -- DDR3L MEMORY DOWNx16 CHA  | 33 -- +1.05V/+1V(NB671GQ-Z)      |
| 14 -- DDR3L MEMORY DOWNx16 CHB  | 34 -- +VCC_CORE(ISL95833)        |
| 15 -- Level Shifter (SOC_EC)    | 35 -- 1.8V/1.35V LDO-1 (G9661)   |
| 16 -- Level Shifter (SOC_DEV)   | 36 -- 1.8V/1V/3.3V LDO-2 (G9661) |
| 17 -- LCD/CCD/DMIC              | 37 -- Thermal protect            |
| 18 -- Google Debug              | 38 -- Power Sequence             |
| 19 -- HDMI                      | 39 -- SMBUS/I2C                  |
| 20 -- WIFI/BT(NGFF)             | 40 -- BTM PWR TREE               |
|                                 | 41 -- Change List                |

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### I2C table

Function	Channel	Read	Write
Touch pad	I2C0	0x67	
Audio codec	I2C1	0x21	0x20
Light sensor	I2C4		

### SMBus table

Function	Channel	Address
Battery	SMB0	
Thermal	SMB2	0x4C

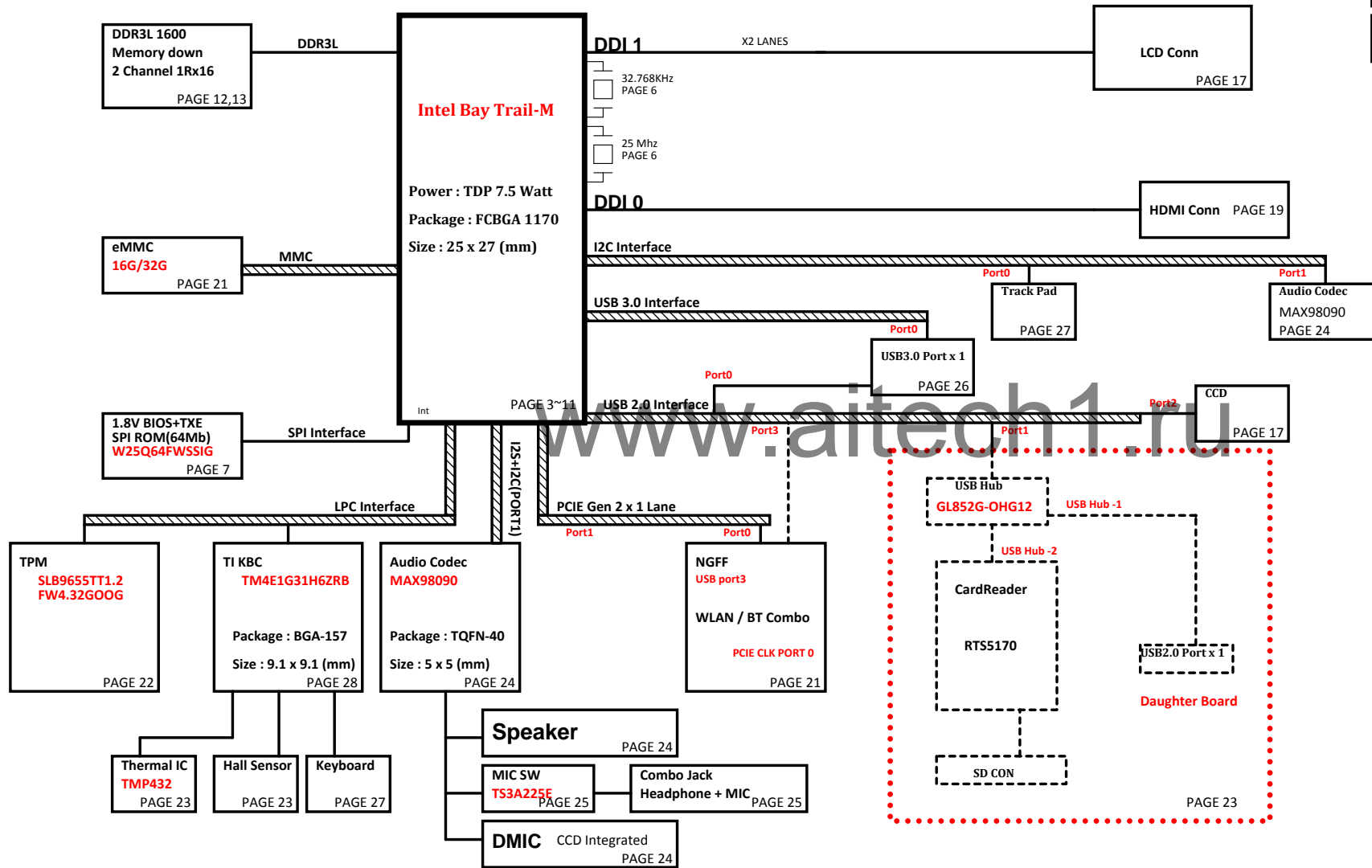
Function	Channel
PP3300_DSW	0x42
PP5000	0x41
PP1350	0x49
PP1050_PCH	0x43
PP1000_PCH	0x47

# ZRU/Vichy

## Intel Bay Trail-M Platform Block Diagram

2

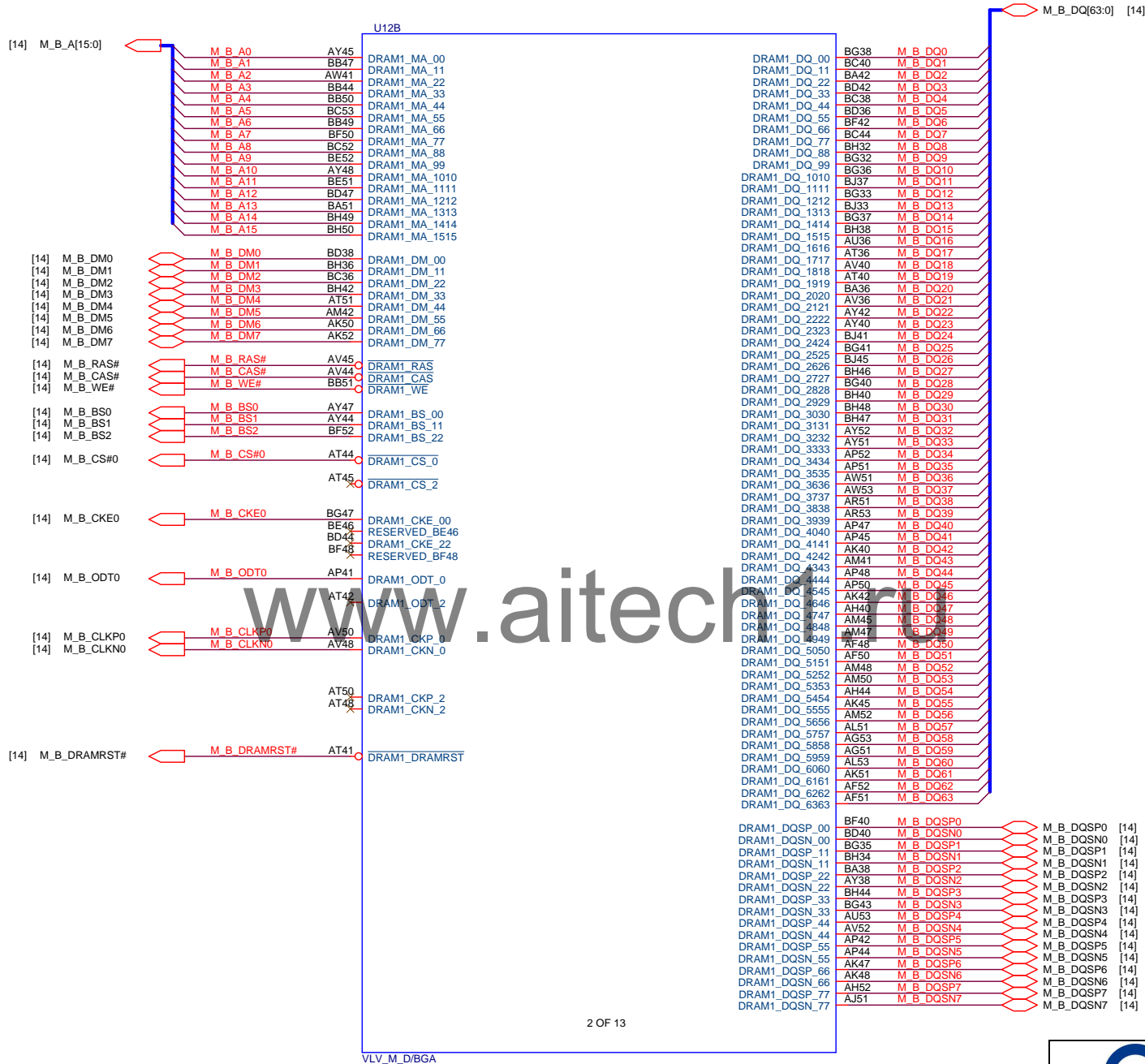
SKUA DC N2830  
AJSR1W4UT02 --CPU(1170P)N2830 2.16G SR1W4(FCBGA)STNBSQ




<b>BQ24717RGRR</b> Battery Charger	<b>TPS51216</b> PP1350
<b>TPS51225</b> PP3300_DSW/PP5000	<b>NB671GQ-Z</b> PP1000_PCH
<b>ISL95833HRTZ-T</b> +VCC_CORE/+VCC_GFX	<b>Thermal Protection Discharger</b>

BOM value option:  
SX@ => SOIX  
NSX@=>none SOIX  
HUB@=>USB HUB  
3G@ => LTE  
GD@ =>Google debug





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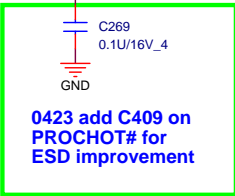


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	<b>Valley 2/9 (DDR8)</b>	1A
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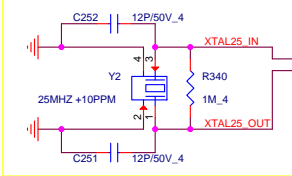


using SoC internal PU

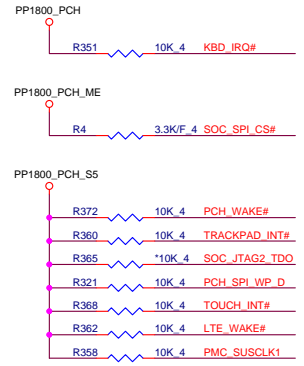




CRYSTAL 25MHZ



2nd BG625000121(HHE)



I2S\_MCLK

[24] I2S\_MCLK

[12] SRT\_CRST#

[12] XDP\_H\_TCK

[12] XDP\_H\_TRST#

[12] XDP\_H\_TMS

[12] XDP\_H\_TDI

[12] XDP\_H\_TDO

[12] XDP\_H\_PRDY#

[12] XDP\_H\_PREQ#\_C

[28] KBD\_IRQ#

[27] TRACKPAD\_INT#

[15] SOC\_KBC\_SMI

[24] MUX\_AUD\_INT1#

[16] WIFI\_DISABLE#

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

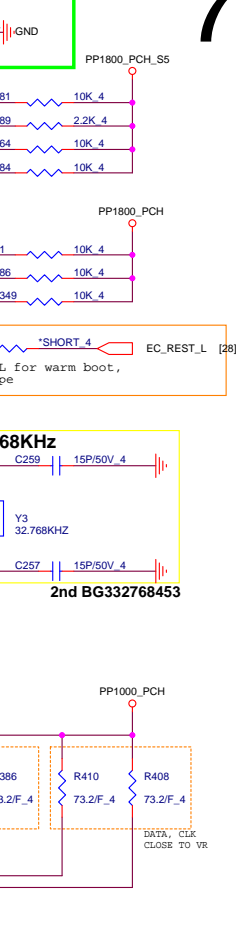
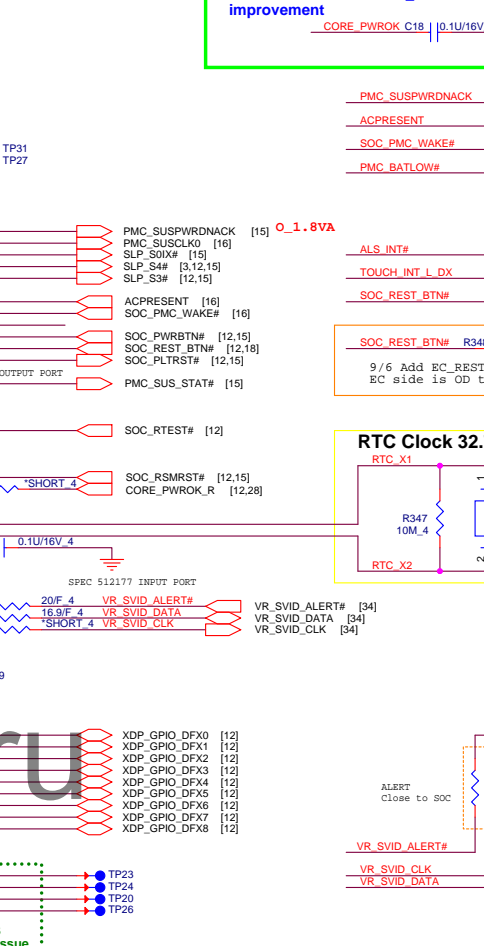
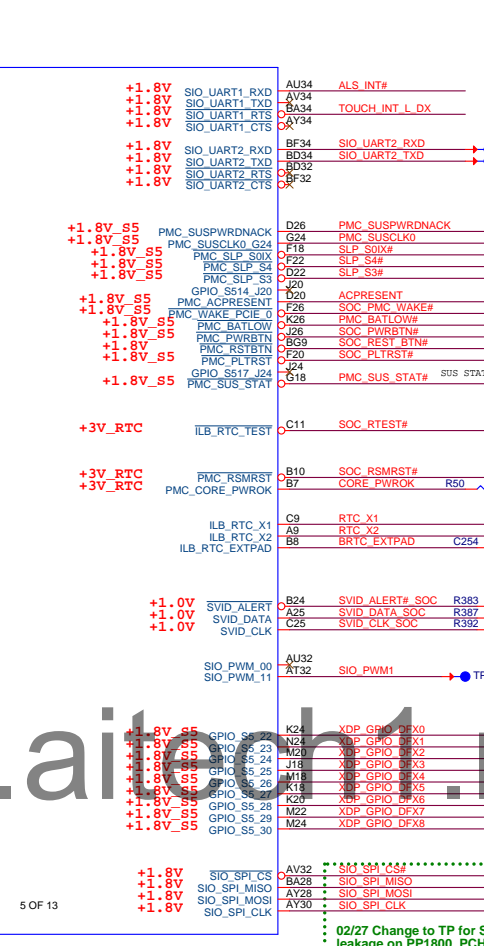
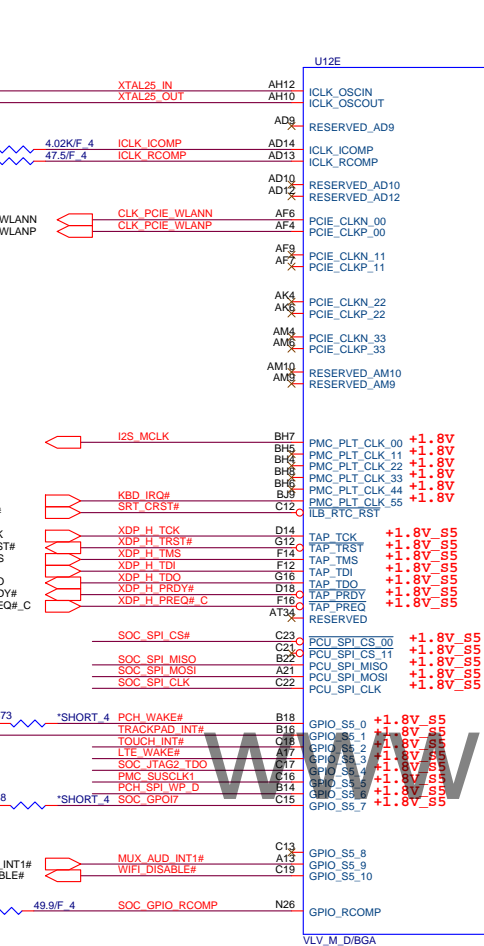
[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

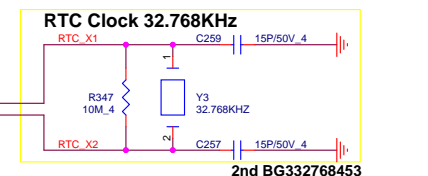
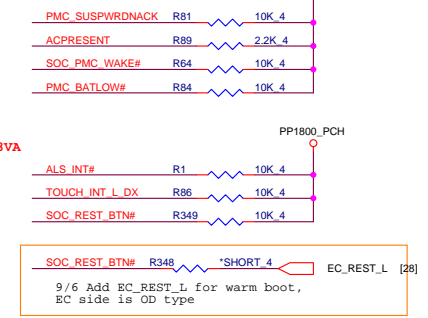
[16] R83 49.9/F\_4

[16] R83 49.9/F\_4

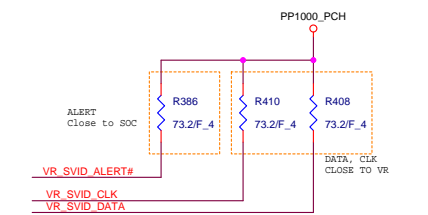
[16] R83 49.9/F\_4



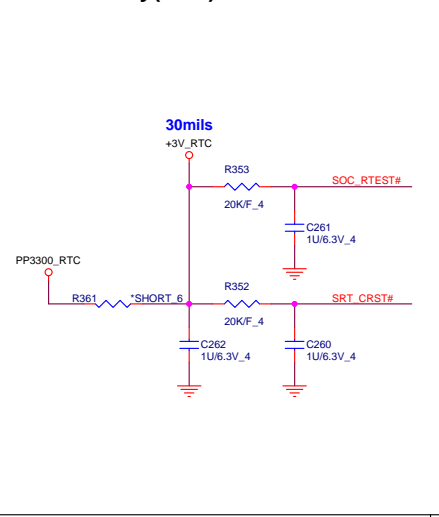
0423 add C408 on CORE\_PWROK for ESD improvement  
CORE\_PWROK C18 0.1U/16V\_4 GND



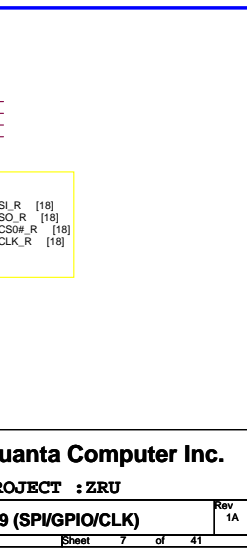
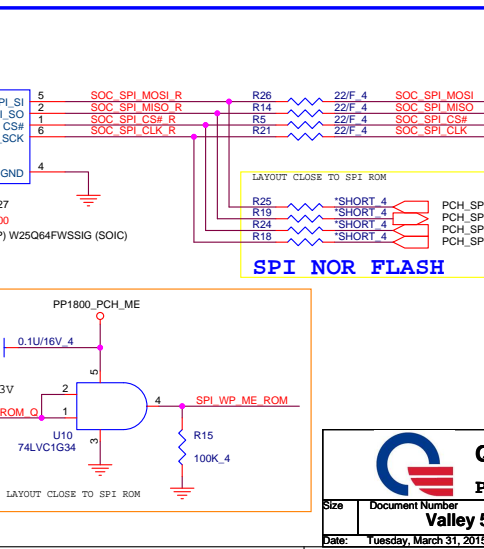
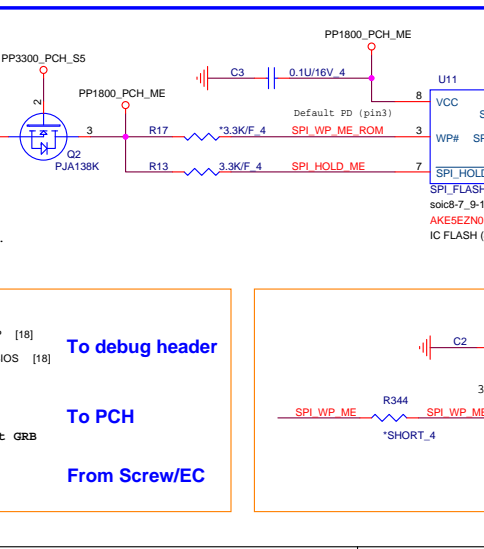
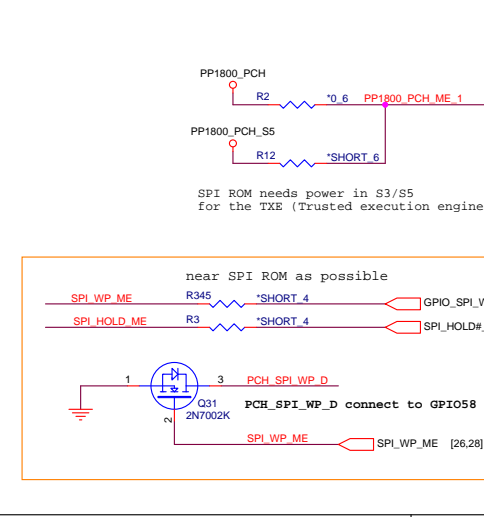
2nd BG332768453



RTC Circuitry(RTC)



SPI\_FLASH



RAM ID

PP1800\_PCH\_S5

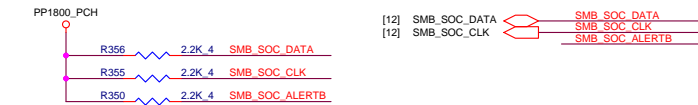
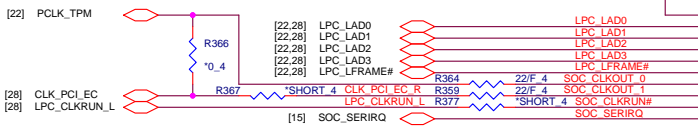
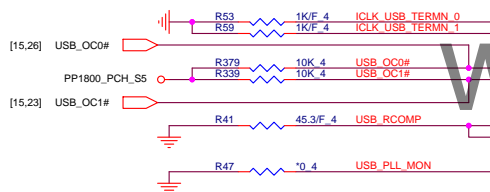
R323 1K\_4 RAM ID0 R319 1K\_4

R324 1K\_4 RAM ID1 R320 1K\_4

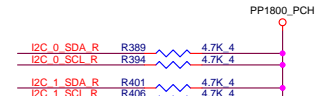
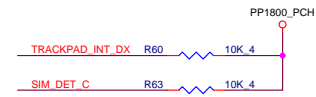
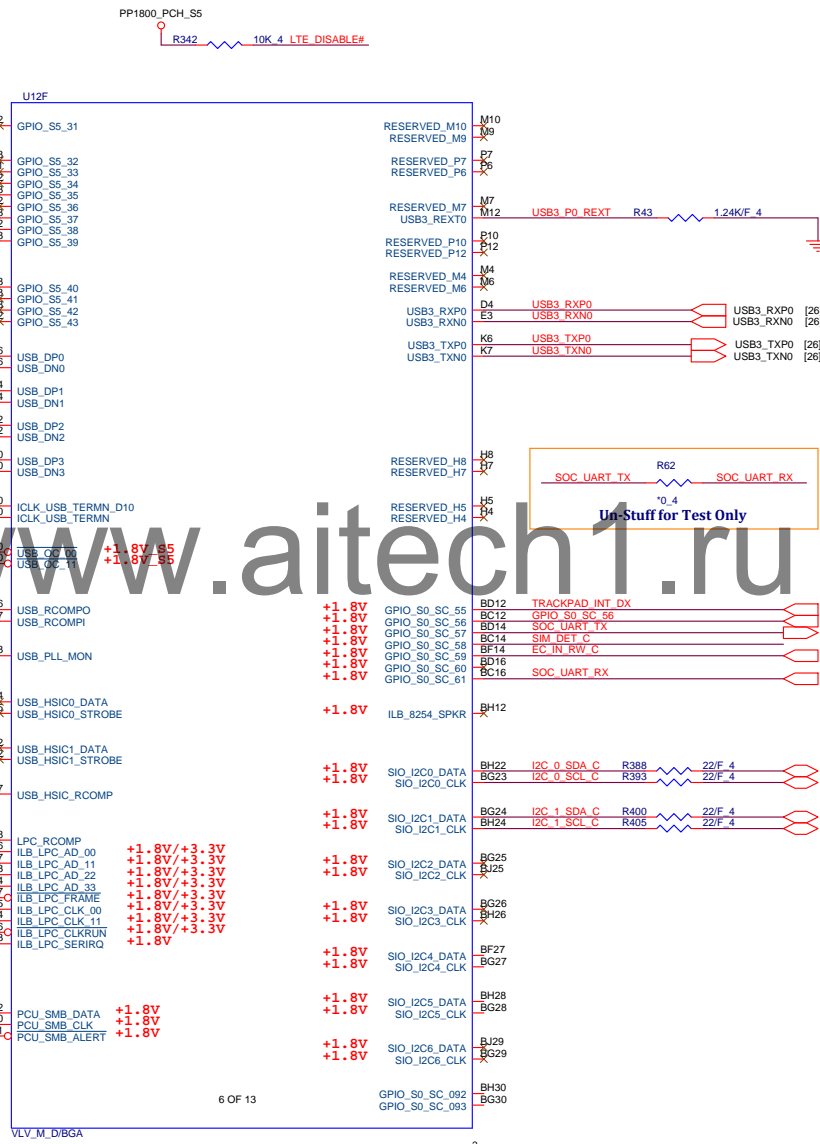
R329 1K\_4 RAM ID2 R318 1K\_4

R341 1K\_4 RAM ID3 R328 1K\_4

12/27 Reserve RAM ID3 for memory BOM option.



GND, R369, \*0.4, SOC\_CLKRUN#

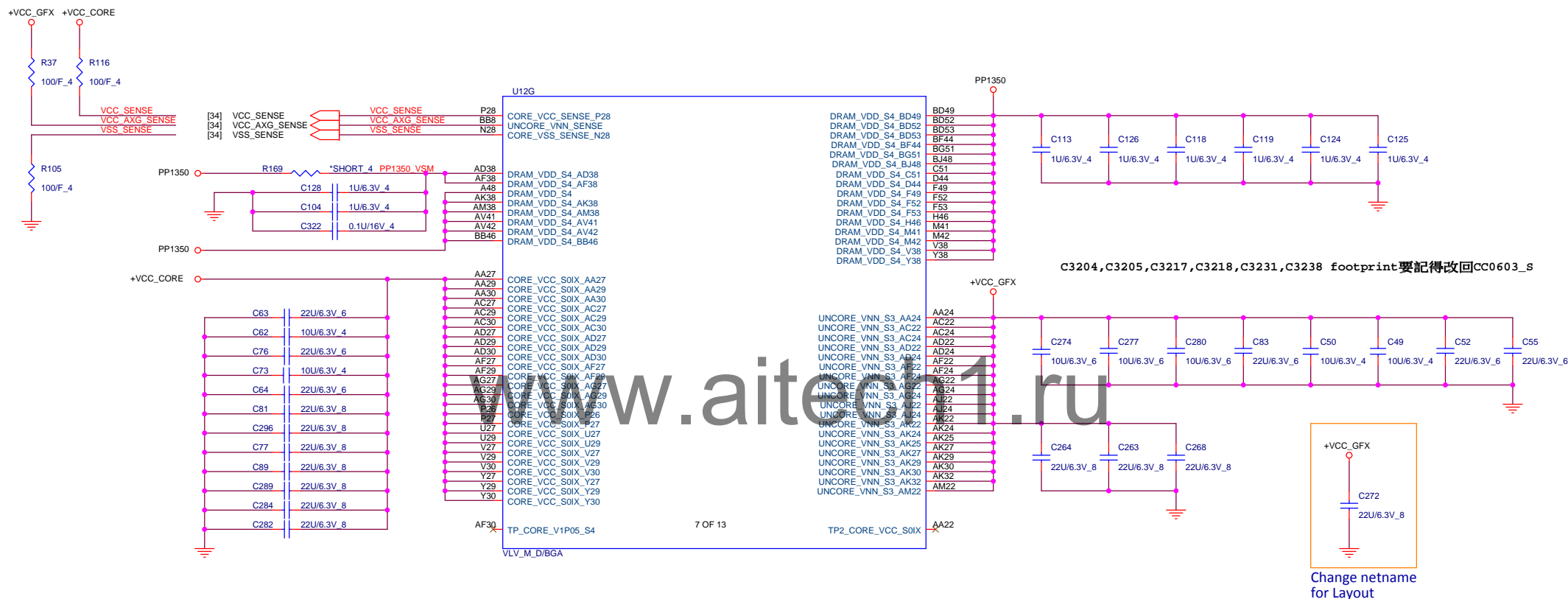


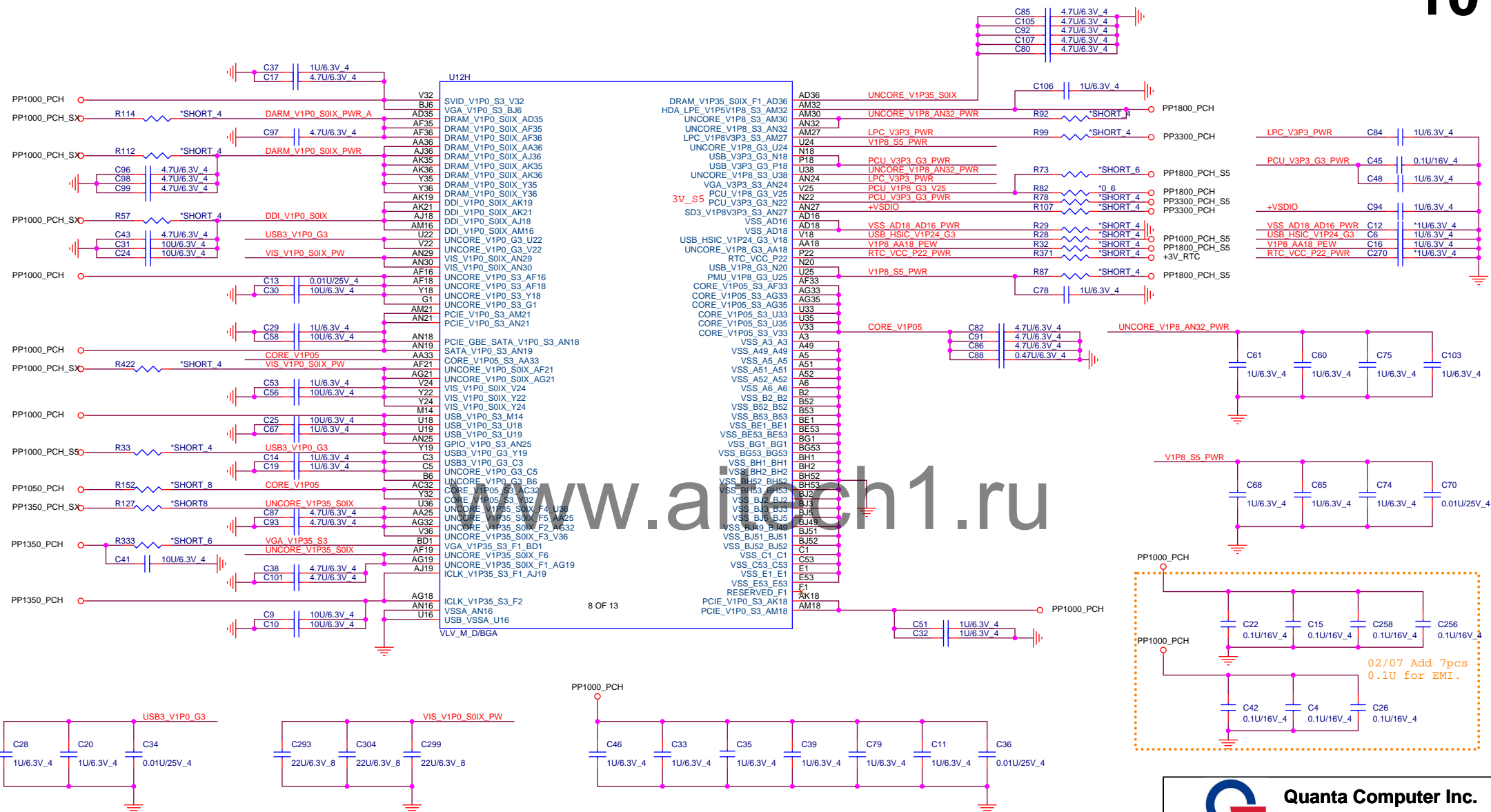


1031 for layout suggestion by intel,  
VSS\_AXG\_SENSE didn't connect to VSS\_SENSE,  
will connect the GND via near VCC\_AXG\_SENSE

1031 for layout, add 0hm between  
GND and VSS\_AXG\_SENSE

[34] VSS\_AXG\_SENSE  R35  \*SHORT 4 







12



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	<b>CPU XDP / APS</b>	<b>1A</b>
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BYTE2\_16-23

BYTE1\_8-15

BYTE0\_0-7

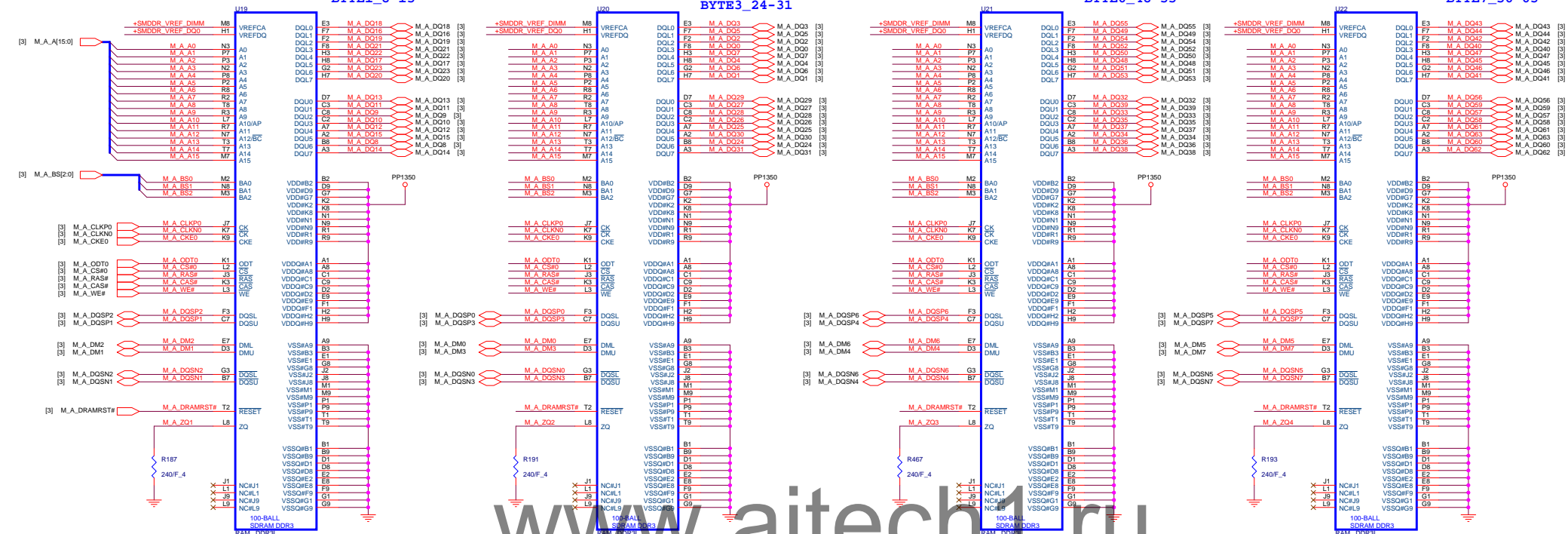
BYTE3\_24-31

BYTE4\_32-39

BYTE6\_48-55

BYTE5\_40-47

BYTE7\_56-63



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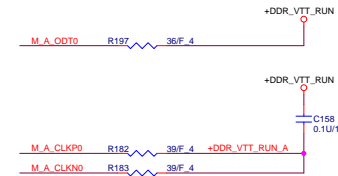
Distributed around all DRAM devices (CHA and CHB)

Place these Caps near each X16 Memory Down

1205 add 0.1uFx2 on PP1350 for EMI request

Place these Caps near Memory Down CA &amp; DQ pin

+DDR\_VTT\_RUN



+DDR\_VTT\_RUN

M1 solution

Vref\_CA

+SMDDR\_VREF\_DIMM

R176 4.7K/0.4

C205 0.047u/10V\_4

R178 4.7K/0.4

C150 0.047u/10V\_4

M1 solution

Vref\_DQ

+SMDDR\_VREF\_DQ0

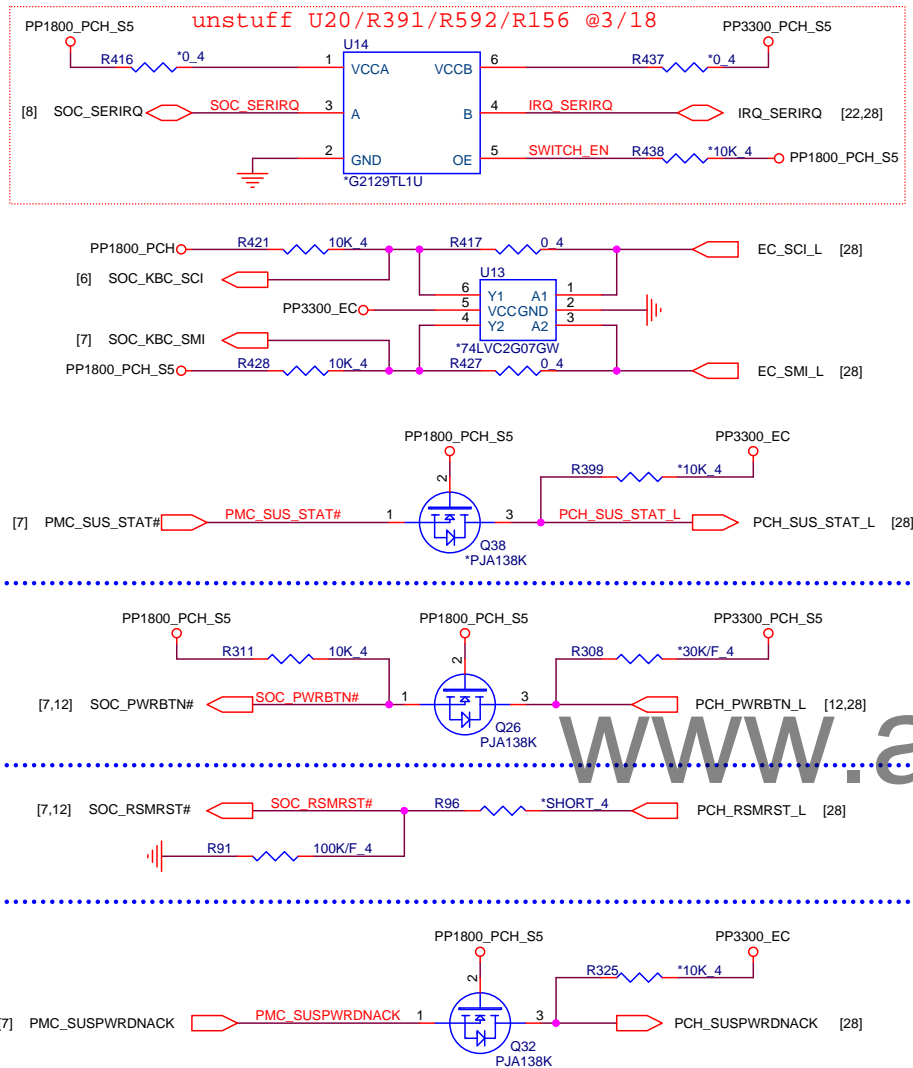
R176 4.7K/0.4

C150 0.047u/10V\_4

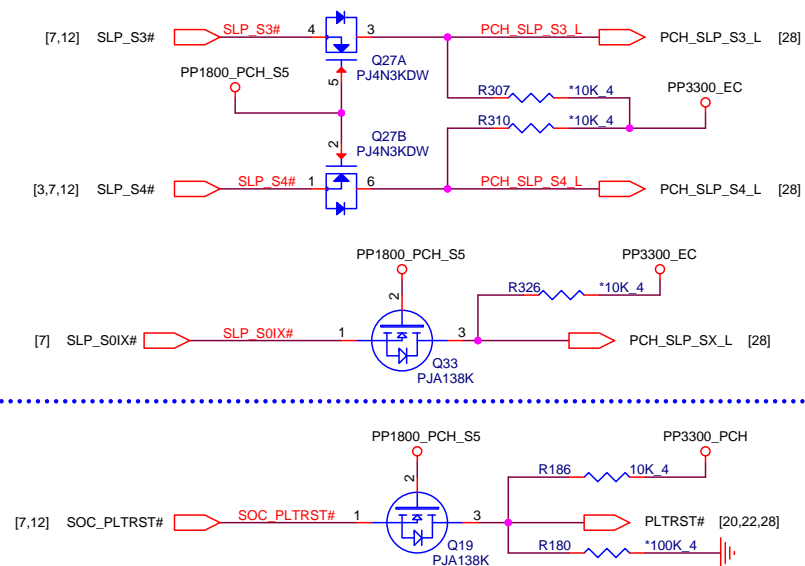
Hynix AKD5JGETW04--H5TC4G63AFR-PBA



## PWRON SEQUENCE

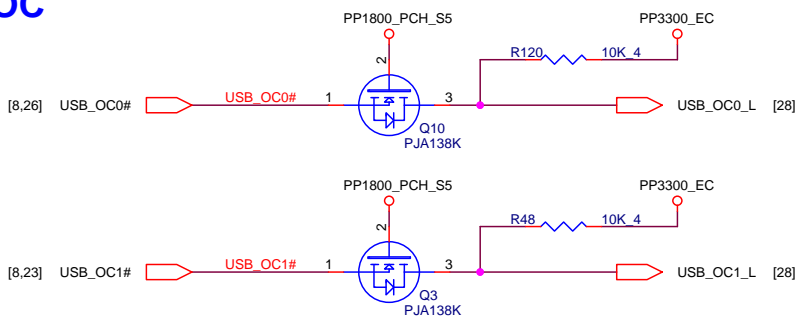


## PWRON SEQUENCE



02/27 Cancel level shift for S3 leakage on PP1800\_PCH issue.

## USB OC



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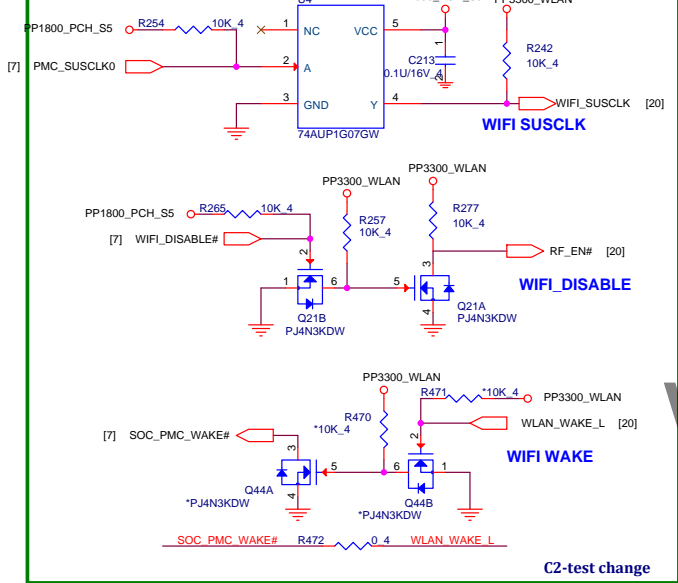
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	Level Shifter (SOC_EC)	1A
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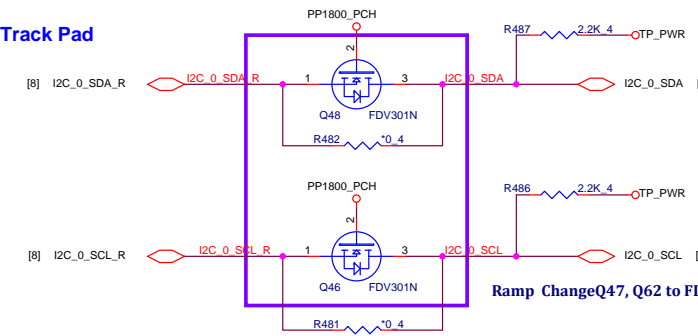


Touch Panel level shift(TPS)

WIFI

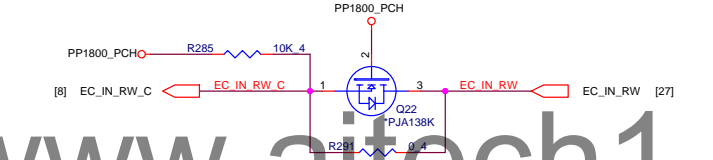


Track Pad

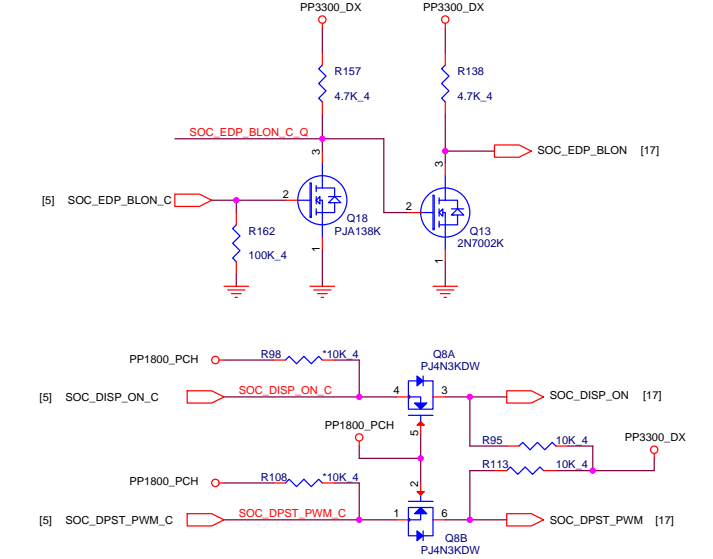


Ramp Change Q47, Q62 to FDSV301N 22u-0326

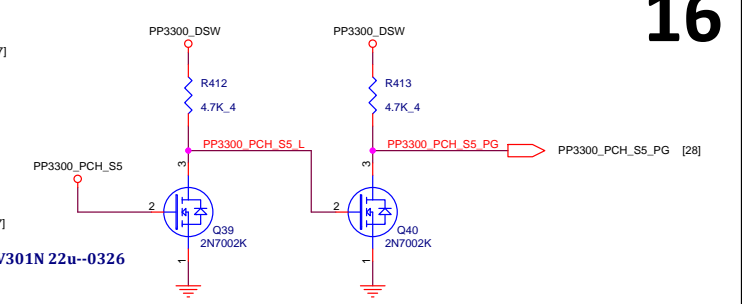
HW RESET



eDP control pin

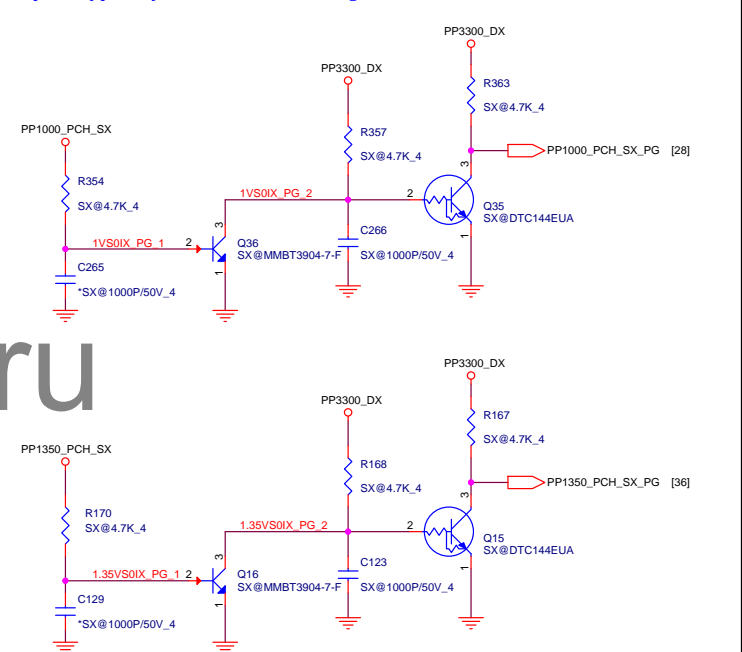


S5 Power Good(+3V\_S5)

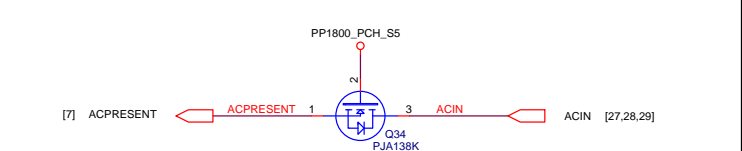


S0iX Power Good

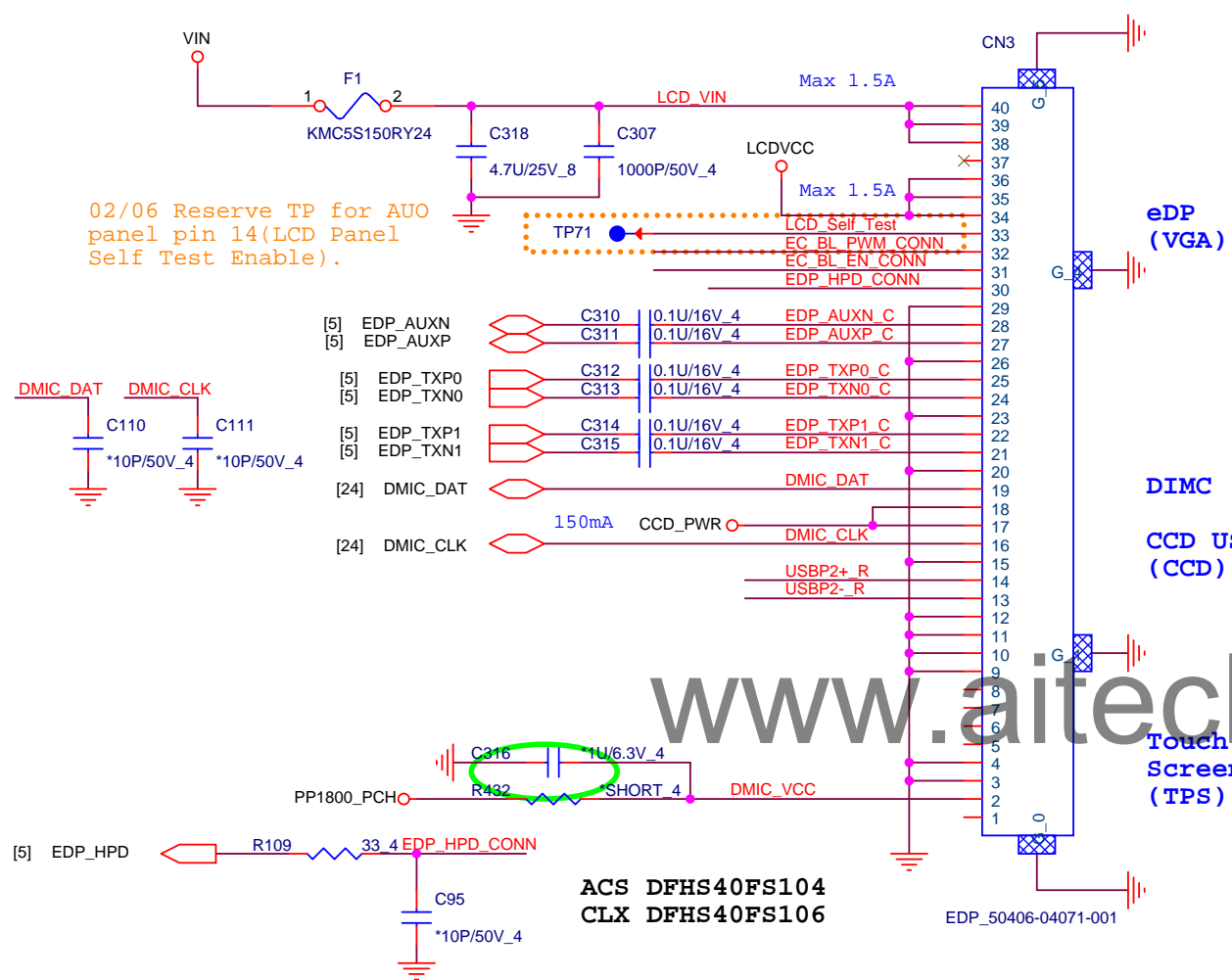
for proto type only, can remove at MP stage if S0ix is not needed



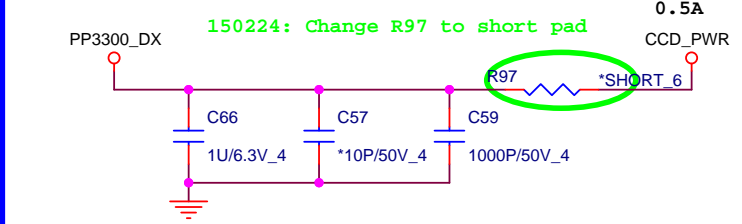
AC Detect



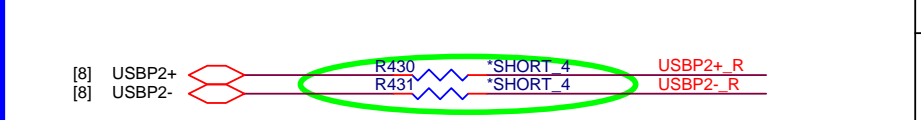
# LCD CONN



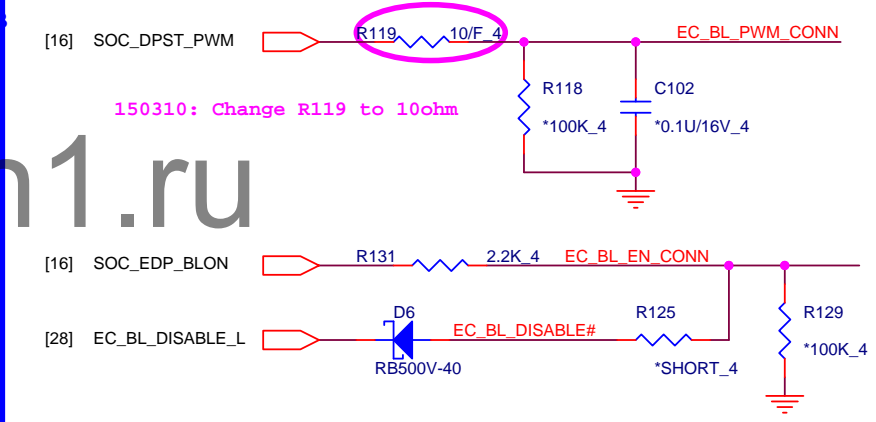
# CCD Power(CCD)



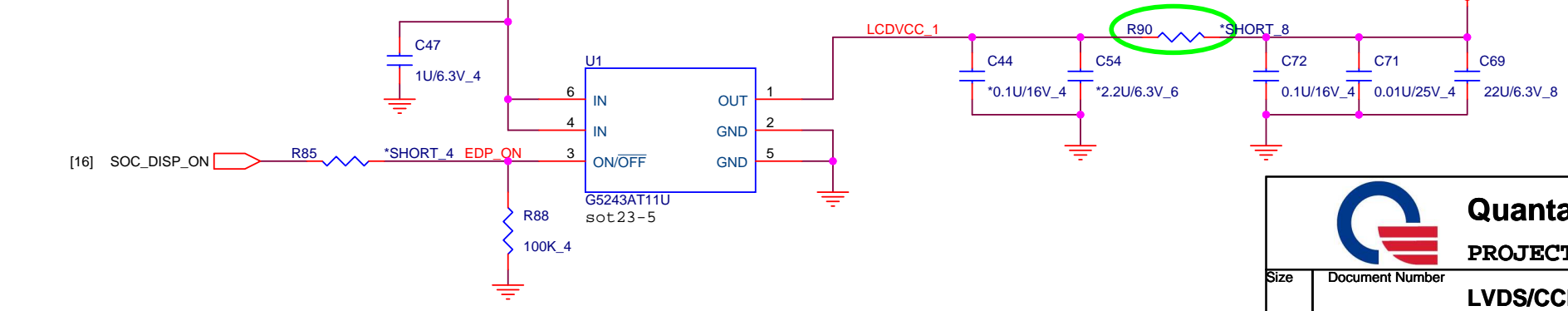
# CCD USB(CCD)



# eDP panel control(LDS)



# eDP Power(LDS)



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**LVDS/CCD/DMIC**

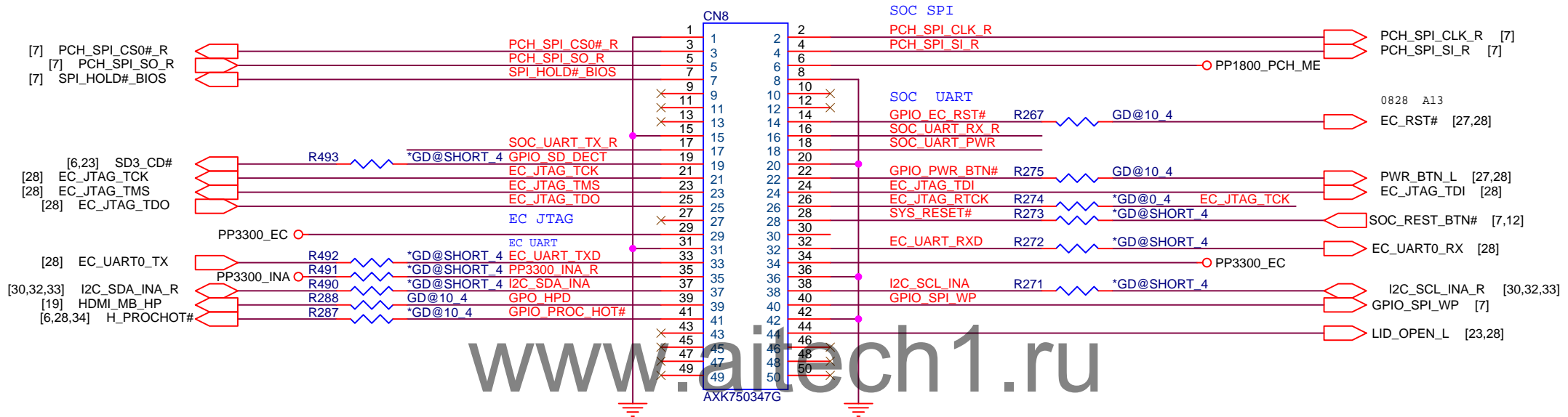
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# GOOGLE Debug Port(MPC)

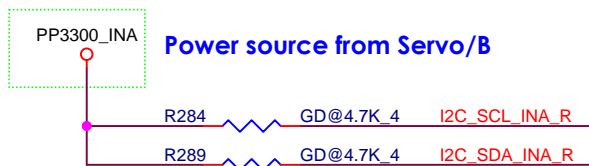
**50 pin BTB is MUST, don't use 42 pin**  
**Socket part number AXK750147G**

PIN7	OD	PIN39	OD	PIN49	OD
PIN14	OD	PIN41	OD	PIN50	OD
PIN19	OD	PIN43	OD		
PIN22	OD	PIN44	OD		
PIN28	OD	PIN45	OD		
PIN30	OD	PIN46	OD		
PIN37	OD	PIN47	OD		
PIN38	OD	PIN48	OD		

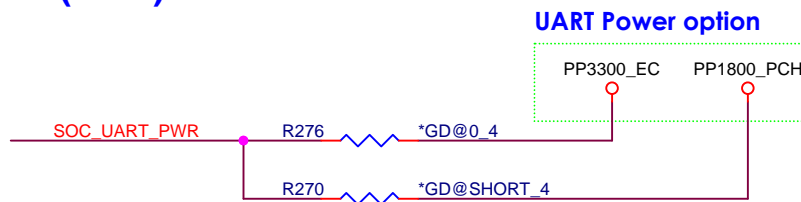
# 18



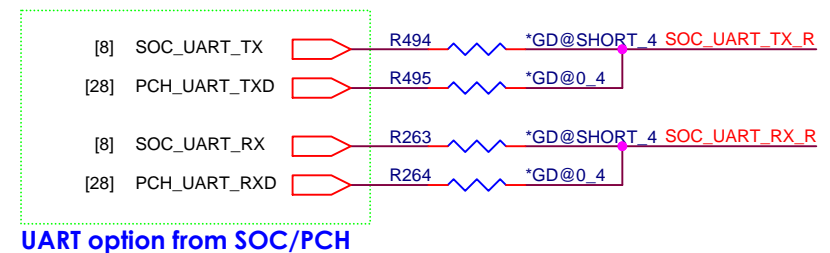
## Servo/B I2C Power(MPC)




## UART Power(MPC)



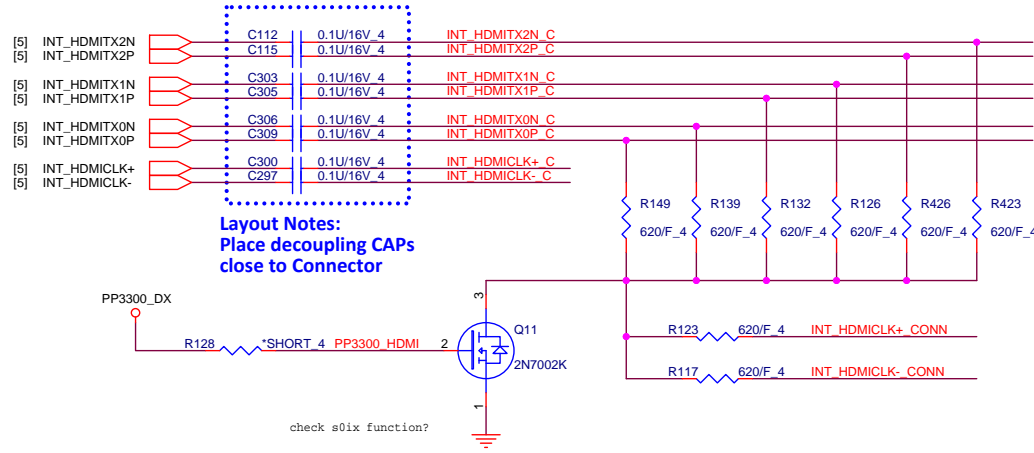
## UART(MPC)



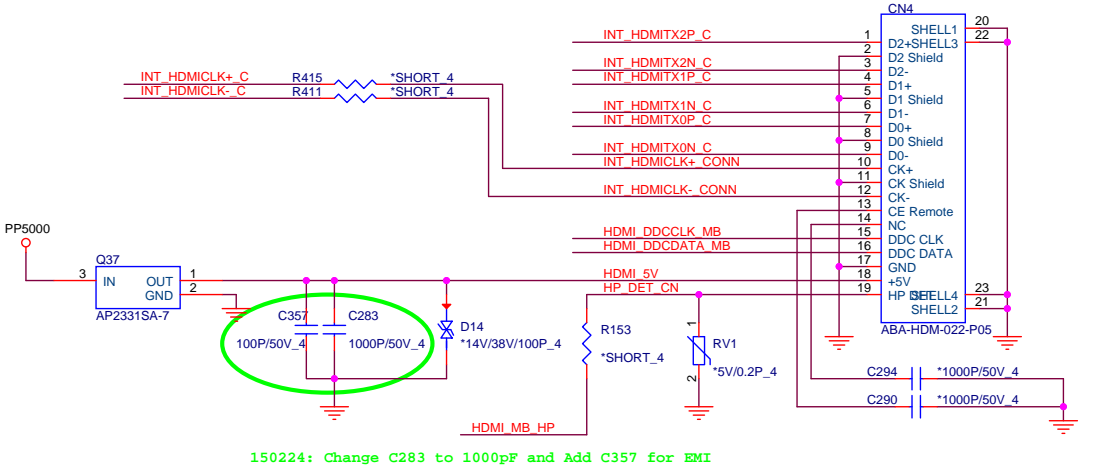
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	<b>Google Debug</b>	1A
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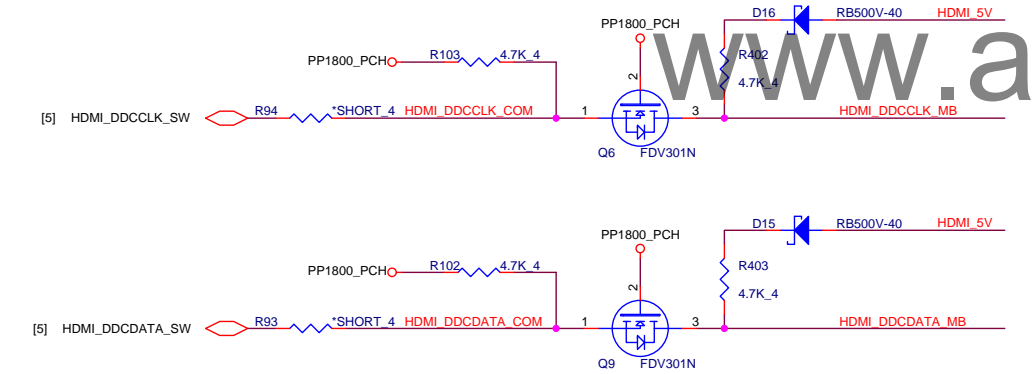
HDMI Cost Reduced level shift (HDM)



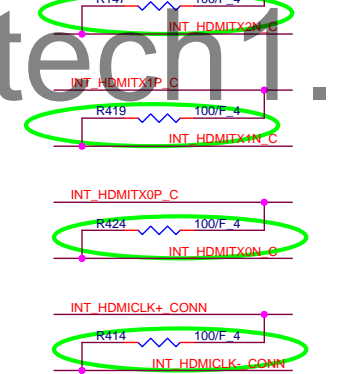
HDMI connector (HDM)



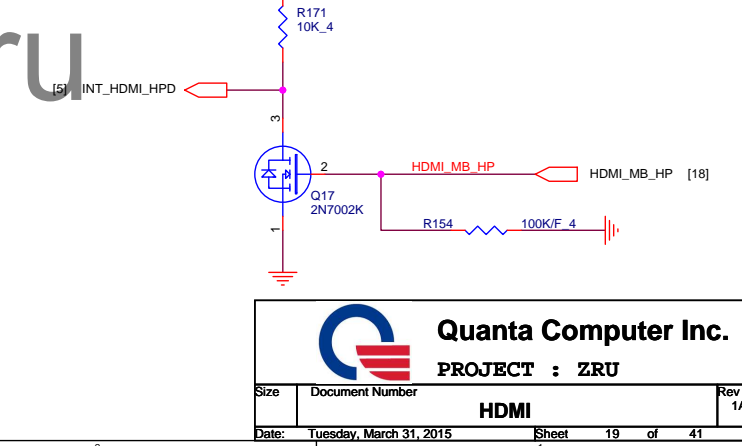
HDMI DDC (HDM)



EMI



HDMI-detect (HDM)



# WIFI/BT COMBO NGFF E KEY(MNC)

20

(Low Active)  
(Low Active)

WLAN\_OFF\_L POWER DOWN LAN CHIP from EC?  
WIFI\_DISABLE\_L disable Antenna from PCH?

[16] RF\_EN#  
[28] WLAN\_OFF\_L  
[15,22,28] PLTRST#  
[16] WIFI\_SUSCLK

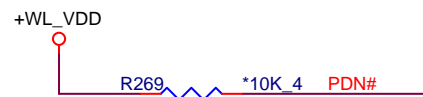
TP51  
TP50  
TP49

NFC\_ANT\_N  
NFC\_ANT\_P  
NFC\_VDDANT  
PIN54: disable Antenna  
PIN52: power down CHIP

RF\_EN  
PDN#  
WLAN\_RST#

TP48  
TP47  
TP46  
TP45

NFC\_WL\_IN  
NFC\_SWP2\_IO  
NFC\_ACTIVE  
NFC Security  
WIFI UART\_RX

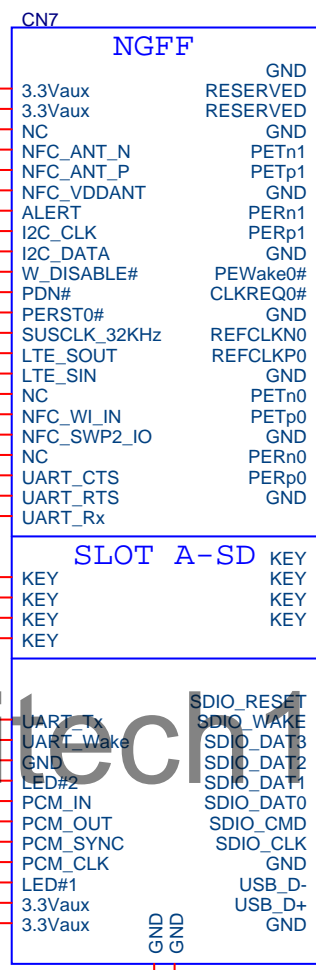


02/05 Remove GPIO  
and reserve TP.

TP44  
TP43  
TP42  
TP41  
TP40  
TP39  
TP38

WIFI UART\_TX  
BT\_LED  
PCM\_IN  
PCM\_OUT  
PCM\_SYNC  
PCM\_CLK  
WLAN\_LED1#

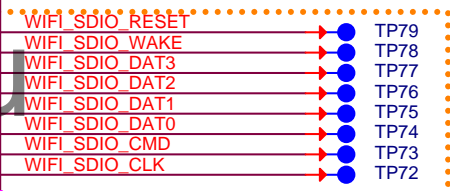
+WL\_VDD



SLOT A-SD  
KEY  
KEY  
KEY  
KEY

SDIO\_RESET  
SDIO\_WAKE  
SDIO\_DAT3  
SDIO\_DAT2  
SDIO\_DAT1  
SDIO\_DAT0  
SDIO\_CMD  
SDIO\_CLK  
GND  
USB\_D-  
USB\_D+  
GND

02/05 Per Customer's  
requirement, add TP on  
WIFI SDIO.

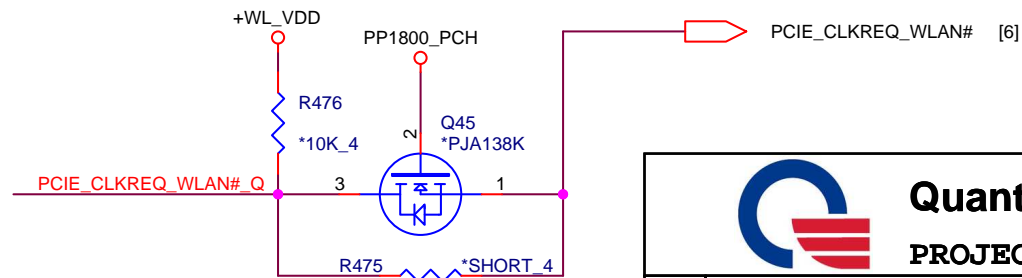
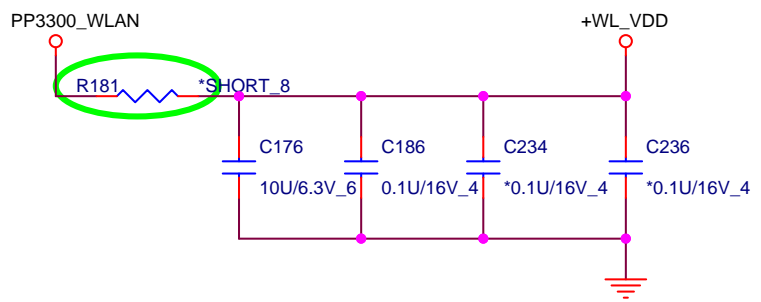


BT

WLAN\_NGFF CONN(Type 2230)\_51745-0750P-005

## WL/BT NGFF Power

150224: Change R181 to short pad

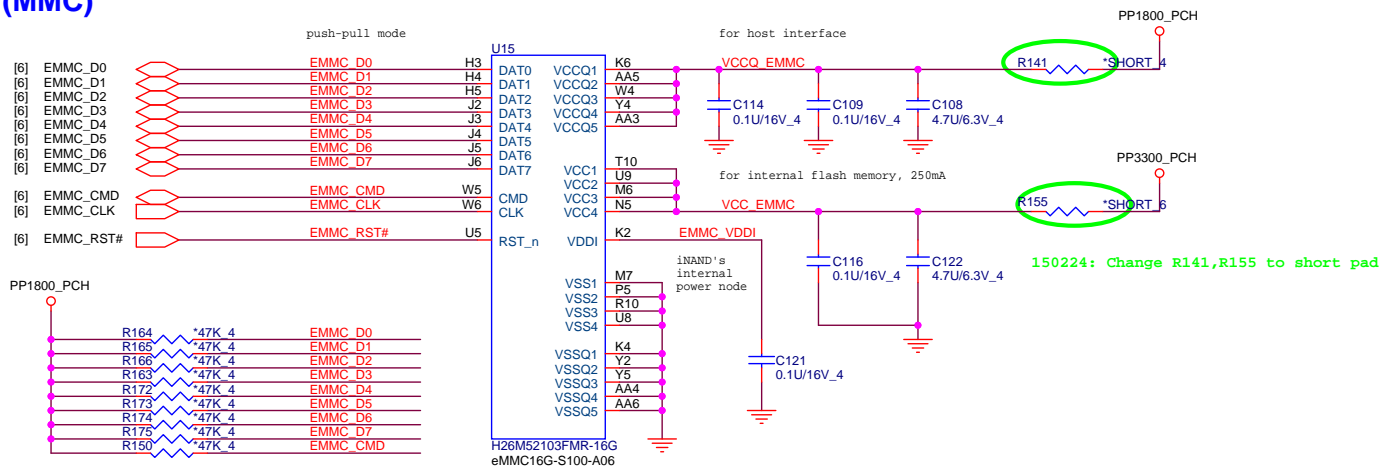


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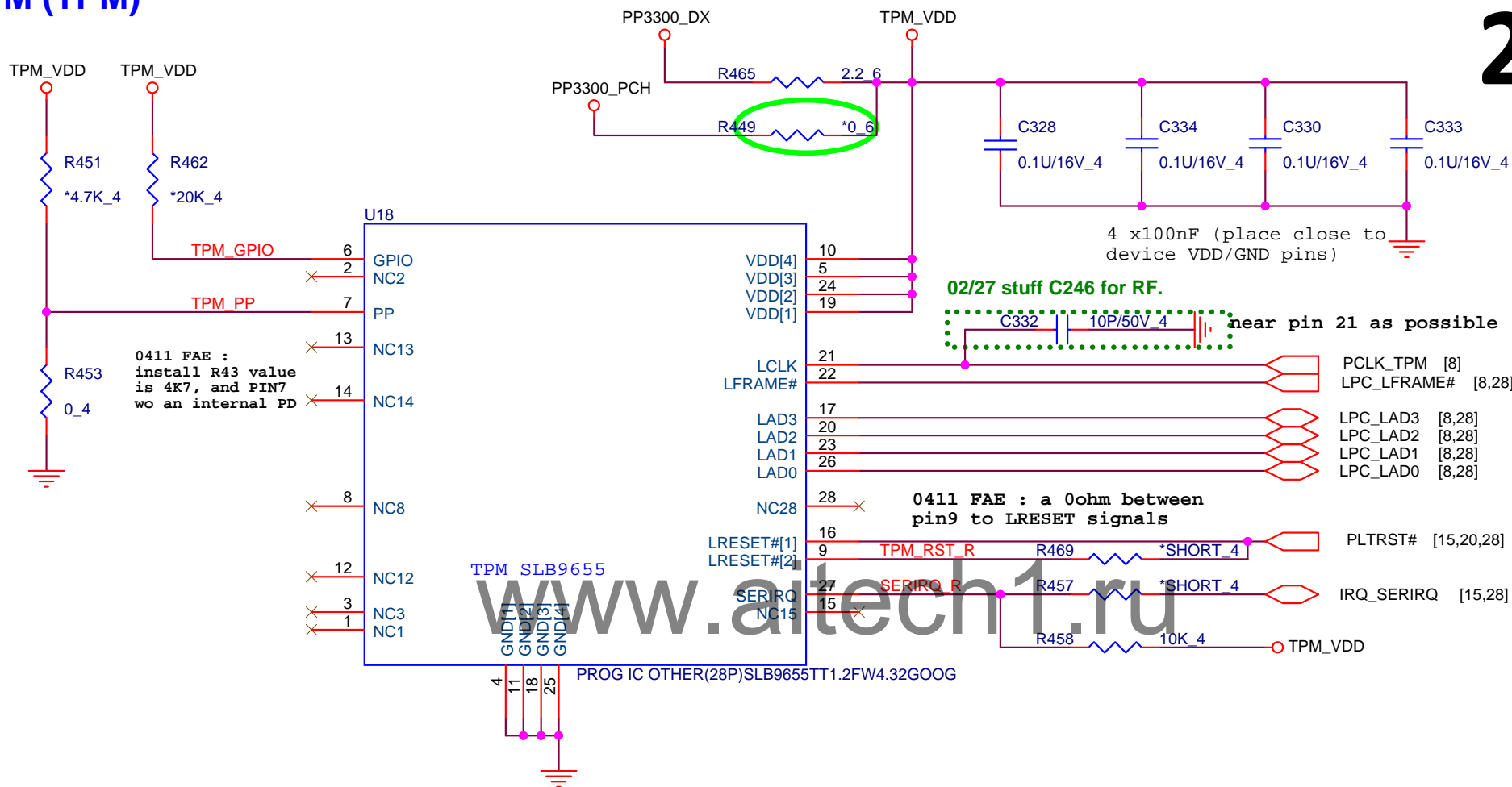
EMMC (MMC)



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# TPM (TPM)

22



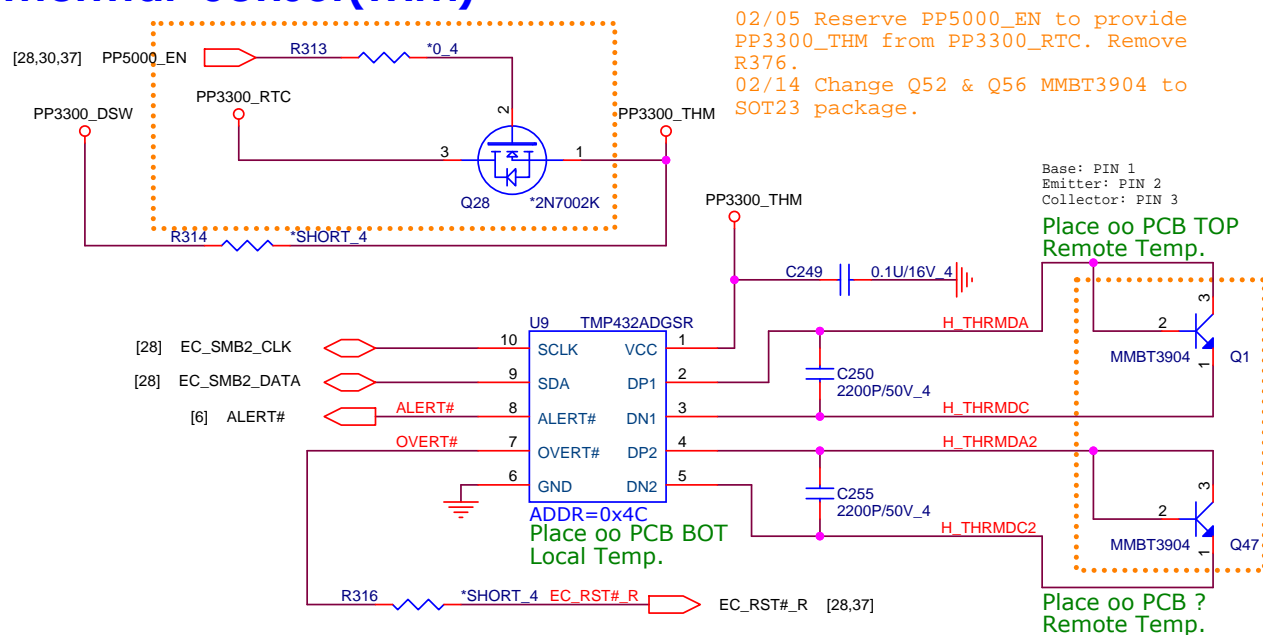
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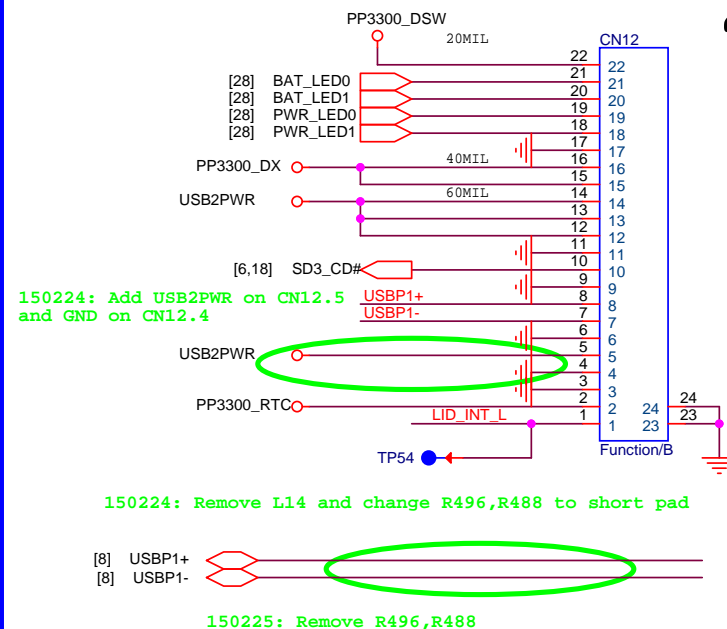
Size	Document Number	Rev
	TPM SLB9655 / LED	1A
Date:	Tuesday, March 31, 2015	Sheet 22 of 41



# Thermal Sensor(THM)

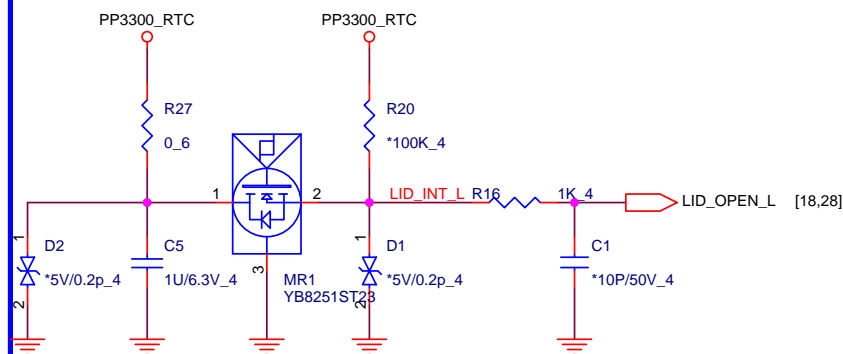
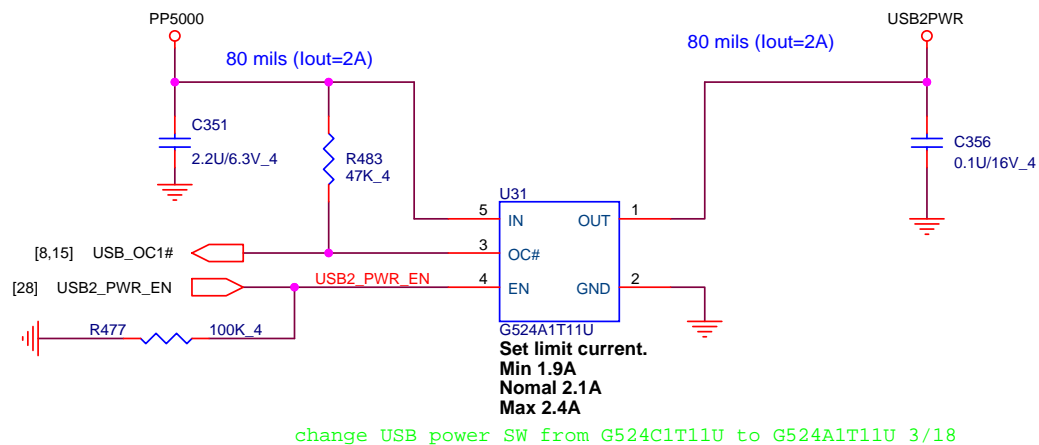


# DB FFC conn 30P



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# Lid Switch (HSR)



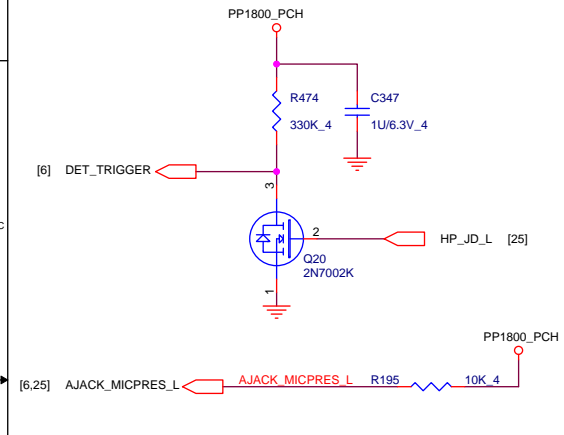
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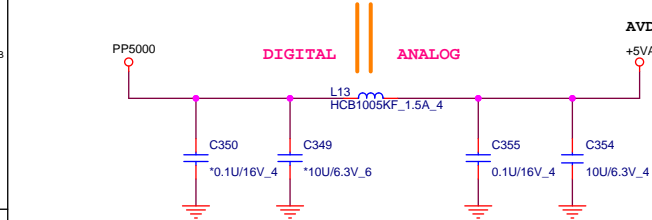
Size	Document Number	Rev
	DB/Thermal sensor/LID	1A
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## AUDIO CODEC (ADO)

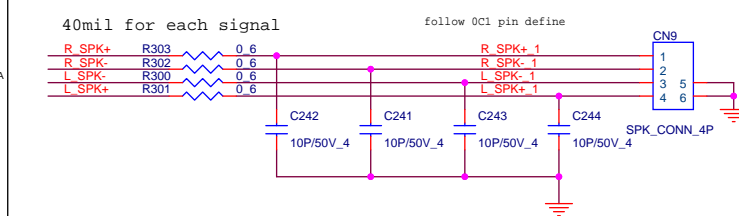
## SOC DET (ADO)



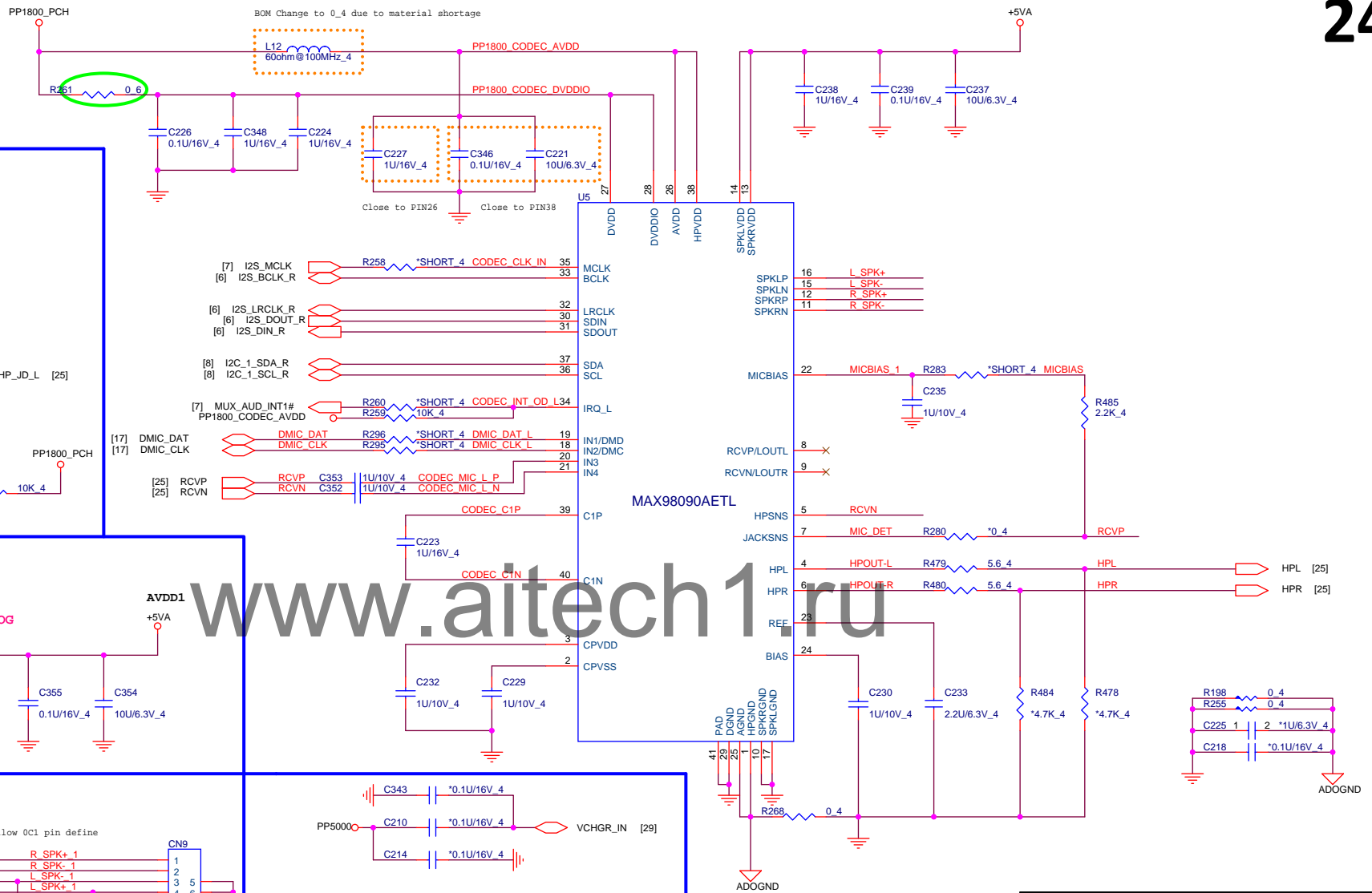
## Codec PWR 5V (ADO)



## Internal Speaker (ADO)



BOM Change to 0\_4 due to material shortage



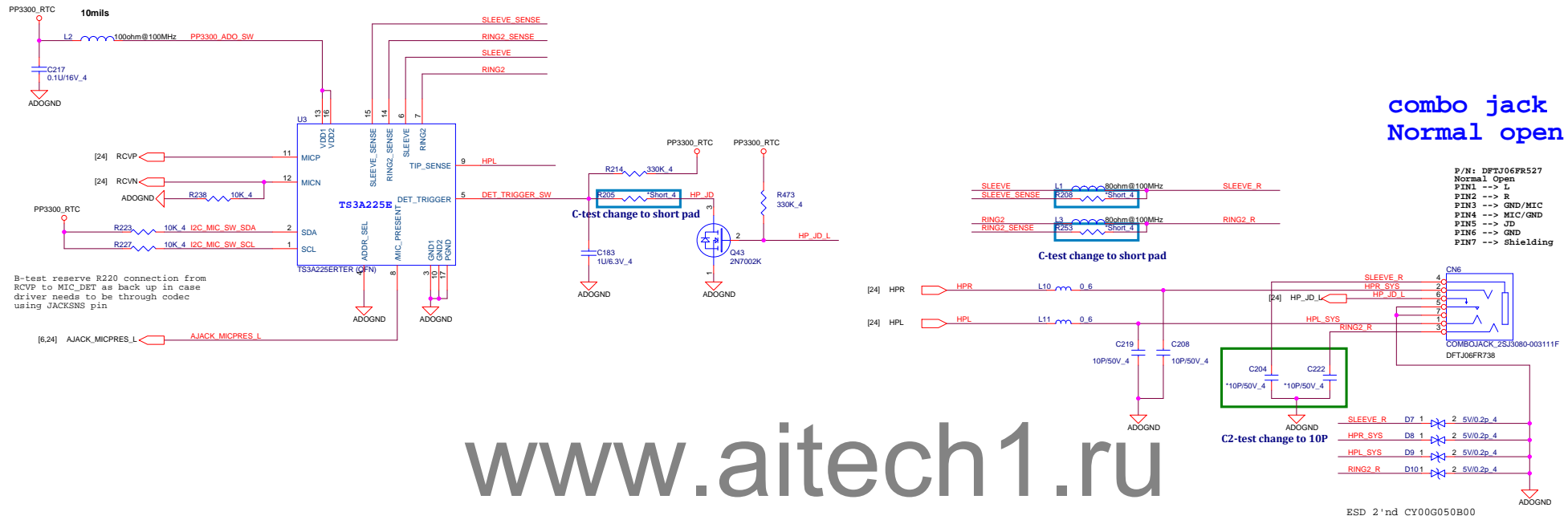
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		1A
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Audio Codec/SPK/DMIC

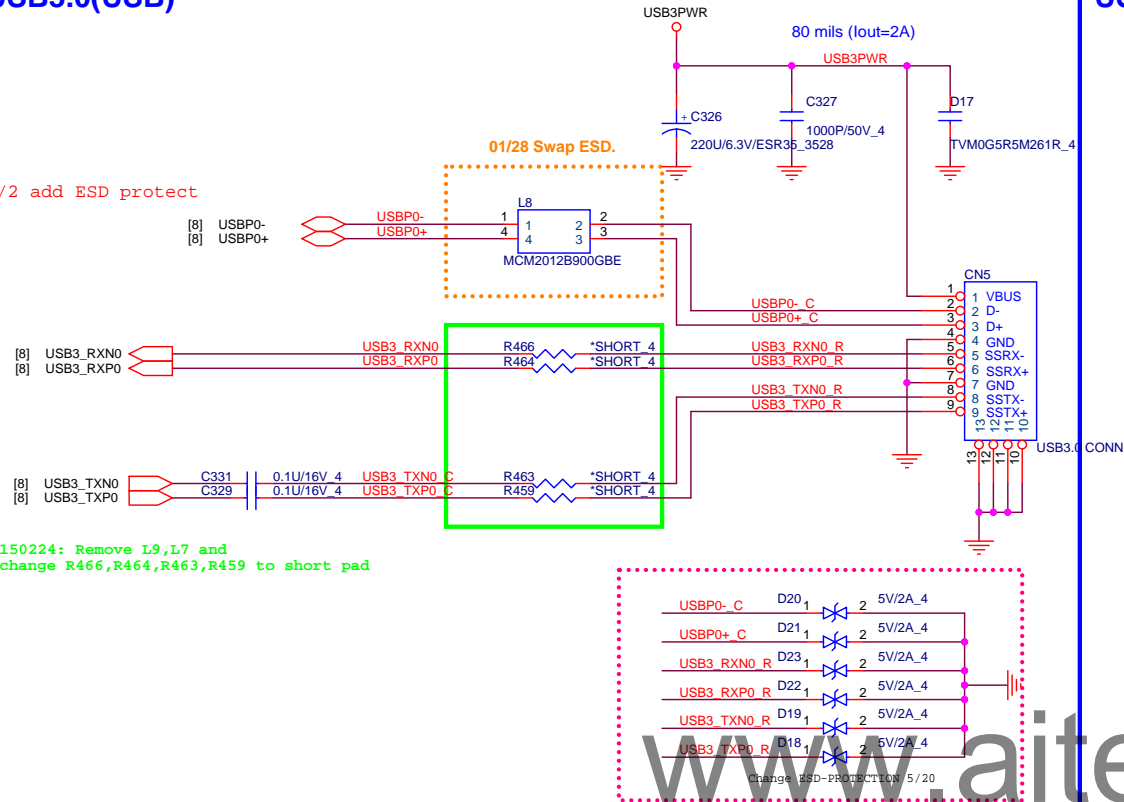
## Audio Headset Switch



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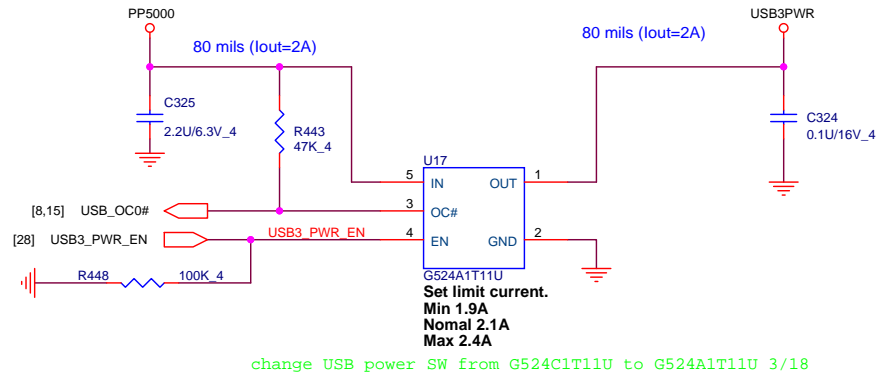
## USB3.0(USB)

1/2 add ESD protect



## USB Switch

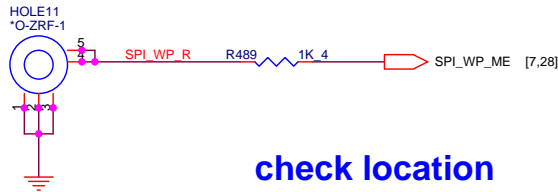
01/28 Change USB power chagreg to power switch.  
Need update footprint.  
02/11 Change USB power switch (U37) from G547F1P81U to G524C1T11U.



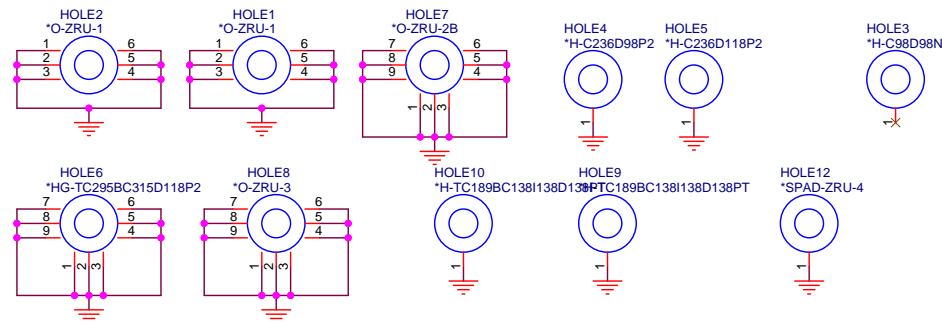
## HOLE(OTH)

02/13 Update hole footprint.

## ROM WP#



## CPU



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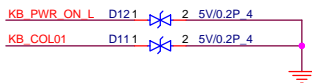
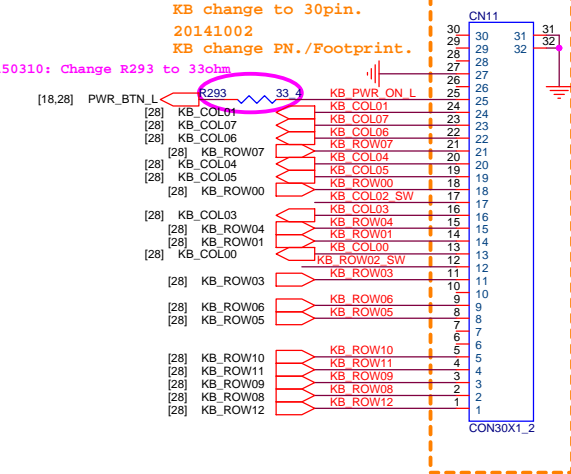
Size	Document Number	Rev
	USB3/Hole	1A

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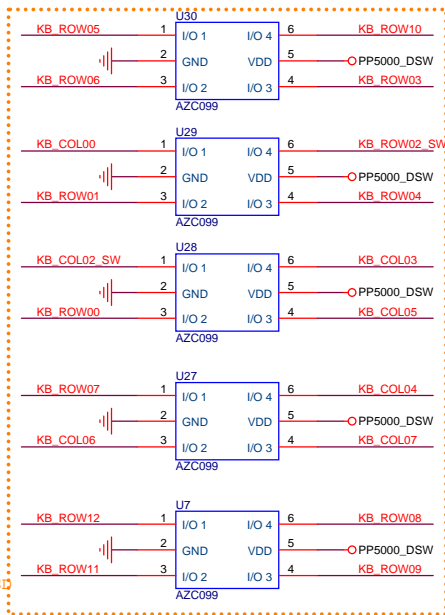
## K/B (KBC)

20140819  
KB change to 30pin.  
20141002  
KB change PN./Footprint.

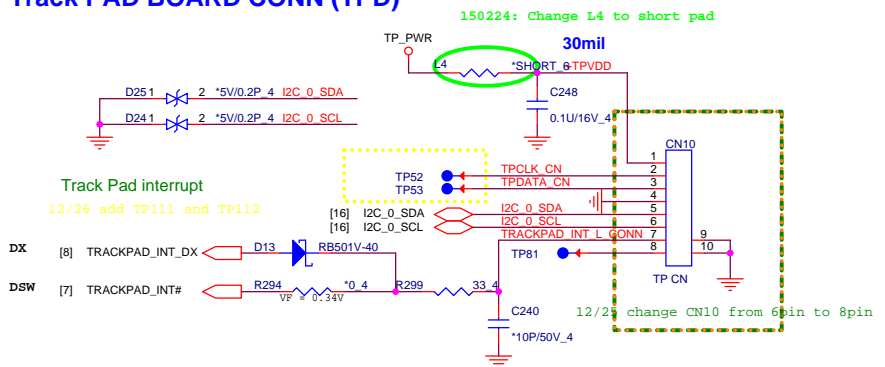
150310: Change R293 to 33ohm



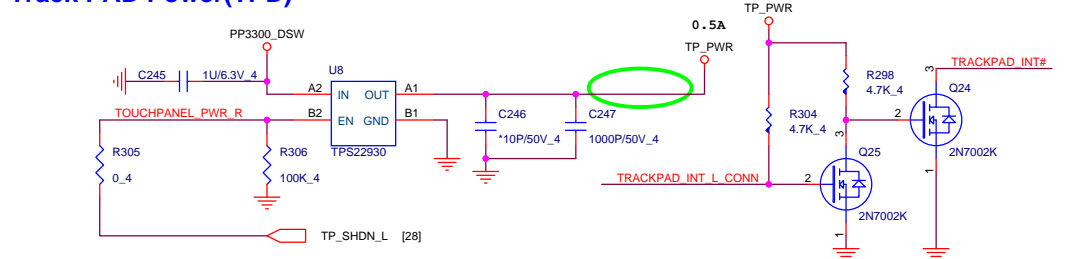
02/05 Change keyboard ESD pin define for routing.



## Track PAD BOARD CONN (TPD)

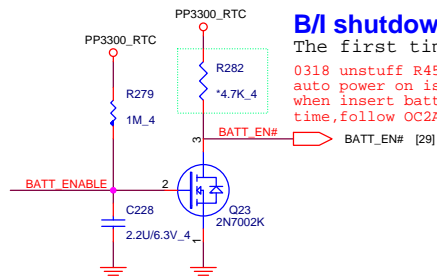


## Track PAD Power (TPD)



## HOLELESS RESET 2-CHIP(KBC)

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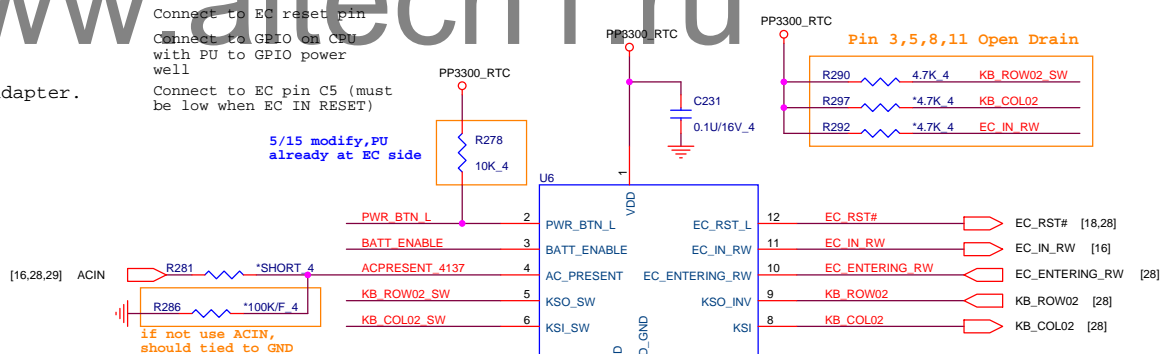
## B/ shutdown function

The first time Power On needs the AC adapter.

0318 unstuff R454 for auto power on issue when insert battery first time, follow OC2A

Connect to EC reset pin  
Connect to GPIO on CPU with PU to GPIO power well  
Connect to EC pin C5 (must be low when EC IN RESET)

5/15 modify, PU already at EC side



02/27 Reset IC needs to change new version, wait for confirm.

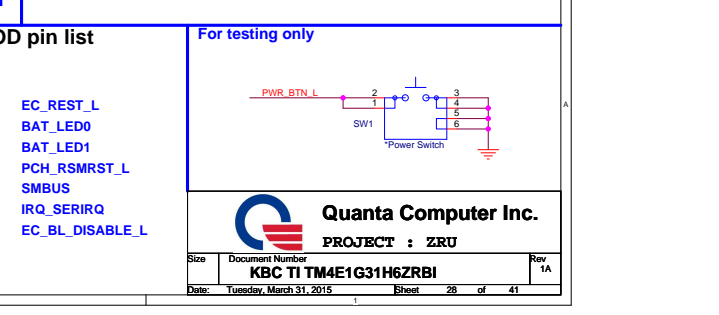
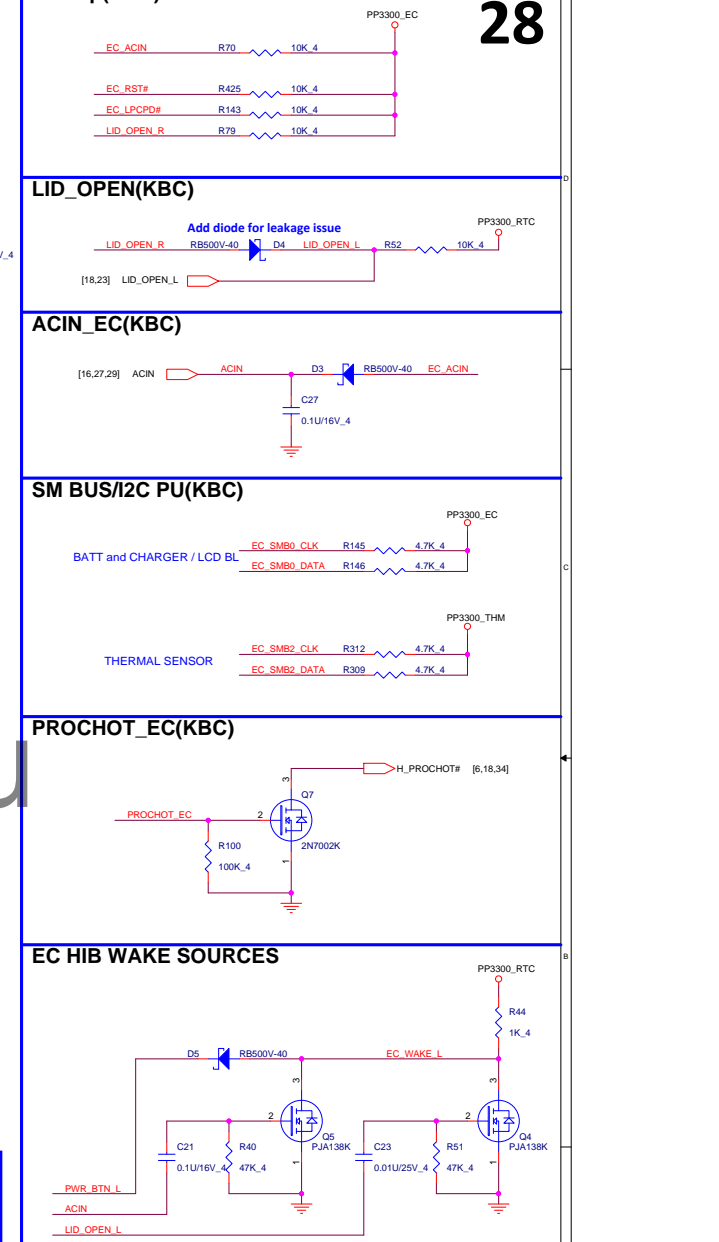
co-layout 4K4108 and 4K4137  
SLG4K4108 (AL004108000)  
SLG4K4137 (AL004137000)  
4K4137 PIN3 is BATT\_ENABLE  
4K4137 PIN4 is AC\_PRESENT

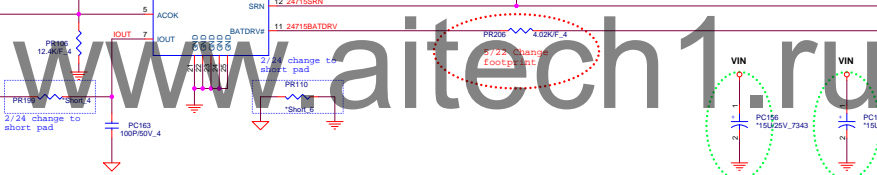


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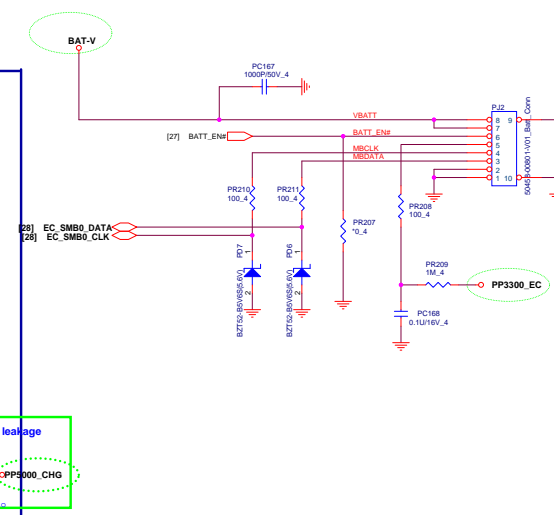
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	KB/TP/HW Reset	1A
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The schematic diagram illustrates the IMVP7 Prochot thermal protection circuit. Key components and their connections include:

- Temperature Sensor:** IMVP7\_PROCHOT (resistor) connected to the input of the comparator.
- Comparator:** PU18A (BA10393F-GE2) with its non-inverting input connected to the sensor and its inverting input connected to a reference voltage.
- Logic Gate:** PU19 (74VHC00) used for signal processing.
- Driver:** PU18B (BA10393F-GE2) driving the S3 LED through a resistor (PR111).
- Resistors:** Various pull-up and pull-down resistors are used throughout the circuit, including PR218, PR226, PR212, PR214, PR216, PR217, PR219, PR220, PR221, PR222, PR223, PR224, PR225, PR226, PR227, PR228, PR229, PR230, PR231, PR232, PR233, PR234, PR235, PR236, PR237, PR238, PR239, PR240, PR241, PR242, PR243, PR244, PR245, PR246, PR247, PR248, PR249, PR250, PR251, PR252, PR253, PR254, PR255, PR256, PR257, PR258, PR259, PR260, PR261, PR262, PR263, PR264, PR265, PR266, PR267, PR268, PR269, PR270, PR271, PR272, PR273, PR274, PR275, PR276, PR277, PR278, PR279, PR280, PR281, PR282, PR283, PR284, PR285, PR286, PR287, PR288, PR289, PR290, PR291, PR292, PR293, PR294, PR295, PR296, PR297, PR298, PR299, PR300, PR301, PR302, PR303, PR304, PR305, PR306, PR307, PR308, PR309, PR310, PR311, PR312, PR313, PR314, PR315, PR316, PR317, PR318, PR319, PR320, PR321, PR322, PR323, PR324, PR325, PR326, PR327, PR328, PR329, PR330, PR331, PR332, PR333, PR334, PR335, PR336, PR337, PR338, PR339, PR340, PR341, PR342, PR343, PR344, PR345, PR346, PR347, PR348, PR349, PR350, PR351, PR352, PR353, PR354, PR355, PR356, PR357, PR358, PR359, PR360, PR361, PR362, PR363, PR364, PR365, PR366, PR367, PR368, PR369, PR370, PR371, PR372, PR373, PR374, PR375, PR376, PR377, PR378, PR379, PR380, PR381, PR382, PR383, PR384, PR385, PR386, PR387, PR388, PR389, PR390, PR391, PR392, PR393, PR394, PR395, PR396, PR397, PR398, PR399, PR400, PR401, PR402, PR403, PR404, PR405, PR406, PR407, PR408, PR409, PR410, PR411, PR412, PR413, PR414, PR415, PR416, PR417, PR418, PR419, PR420, PR421, PR422, PR423, PR424, PR425, PR426, PR427, PR428, PR429, PR430, PR431, PR432, PR433, PR434, PR435, PR436, PR437, PR438, PR439, PR440, PR441, PR442, PR443, PR444, PR445, PR446, PR447, PR448, PR449, PR450, PR451, PR452, PR453, PR454, PR455, PR456, PR457, PR458, PR459, PR460, PR461, PR462, PR463, PR464, PR465, PR466, PR467, PR468, PR469, PR470, PR471, PR472, PR473, PR474, PR475, PR476, PR477, PR478, PR479, PR480, PR481, PR482, PR483, PR484, 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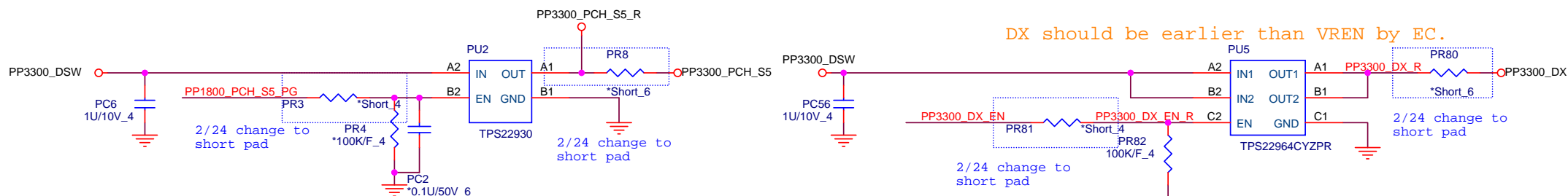
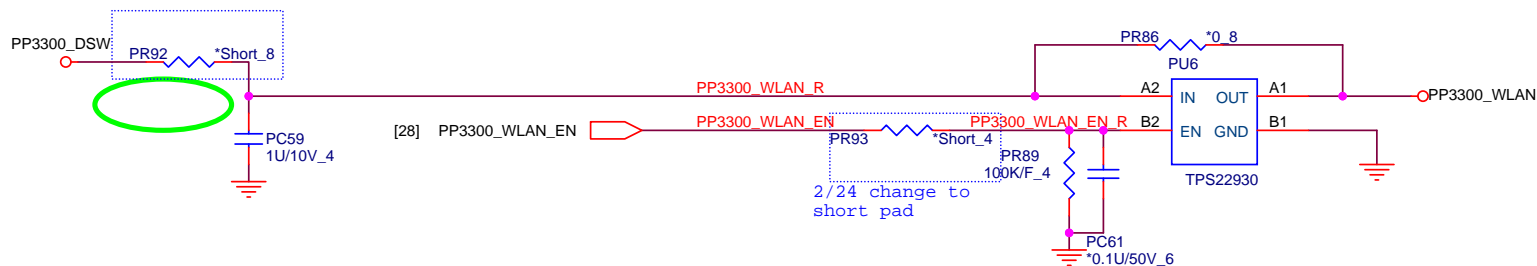
$L(\text{ripple current}) = (9-5) \cdot 5 / (3.3 \cdot 10^{-3} \cdot 0.3 \cdot 10^{-9})$   
 $= 2.2446 \text{ A}$   
 $I_{\text{ocp}} = 5.4 - (2.2446 / 2) = 4.2777 \text{ A}$   
 $V_{\text{th}} = 4.2777 \text{ A} \cdot 14 \text{ m}\Omega + 1 \text{ mV} = 60.878 \text{ mV}$   
 $R(\text{Ilim}) = (60.878 \text{ mV} \cdot 8) / 10 \mu\text{A}$   
 $= 48.7 \text{ k}\Omega$

L(ripple current)  
 $= (9 - 3.3) \times 3.3 / (3.3 \times 0.355 \text{ m}^9)$   
 $\sim 1.7840 \text{ A}$   
 $\text{I}_{\text{ocp}} = 10 - (1.784 / 2) = 9.10798 \text{ A}$   
 $V_{\text{th}} = 9.10798 \text{ A} \times 14 \text{ m}\Omega + 1 \text{ mV} = 128.5117 \text{ mV}$   
 $R(\text{Ilim}) = (128.5117 \text{ mV}^8) / 10 \mu\text{A}$   
 $\sim 102.81 \text{ K}$



[36] PP1800\_PCH\_S5\_PG  
[28] PP3300\_DX\_EN

2/24 change to  
short pad



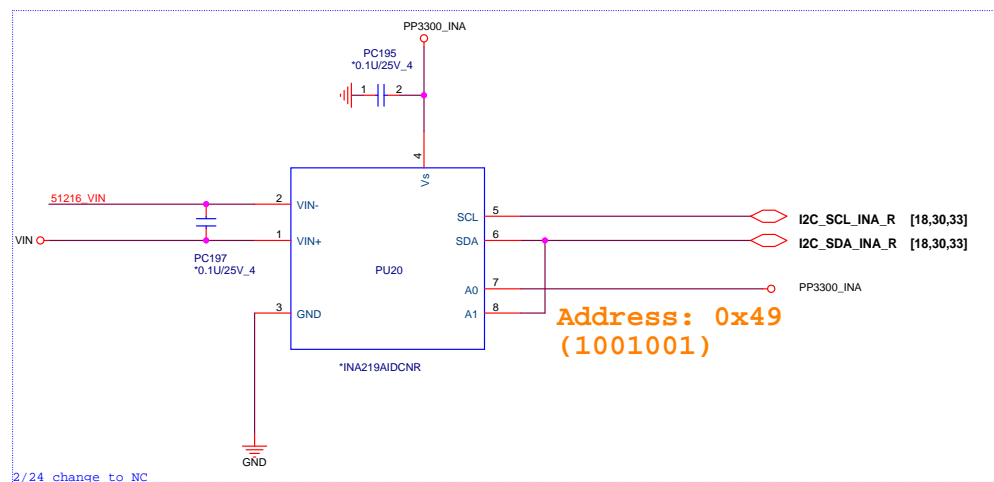
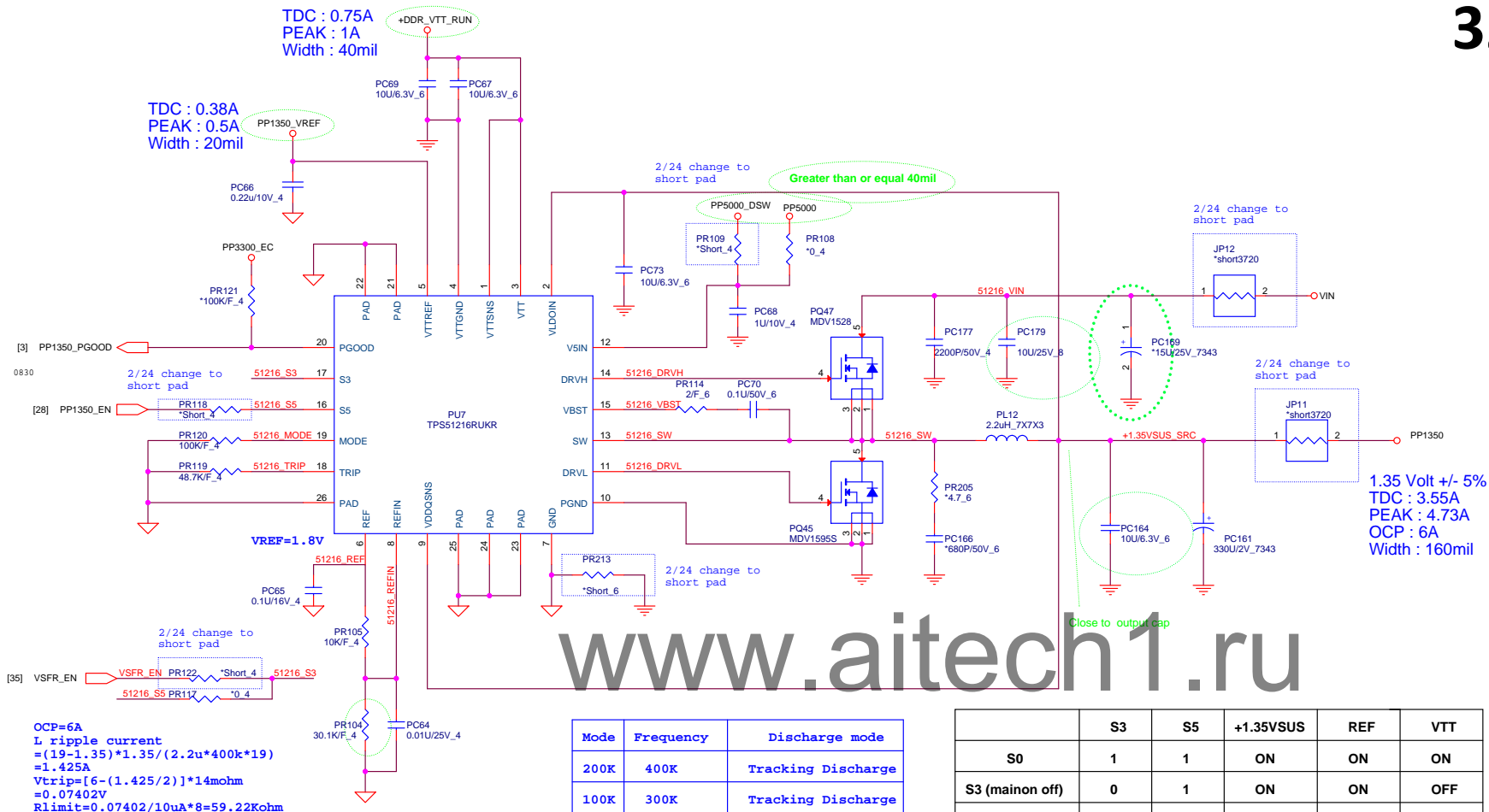
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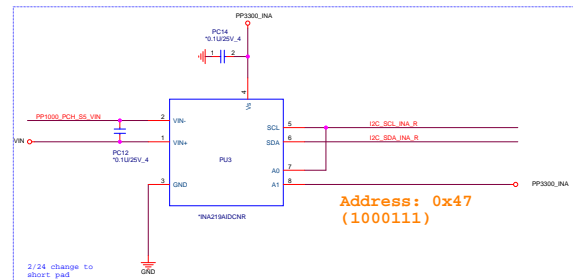
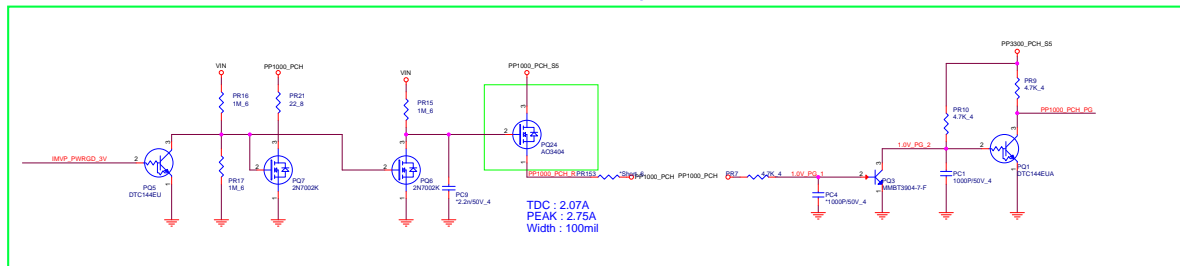
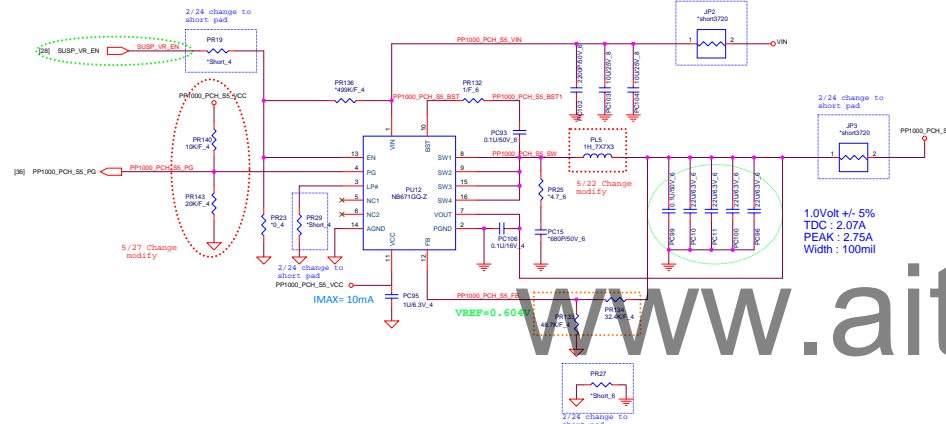


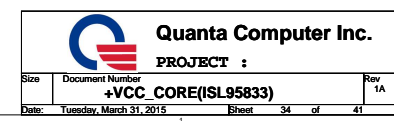
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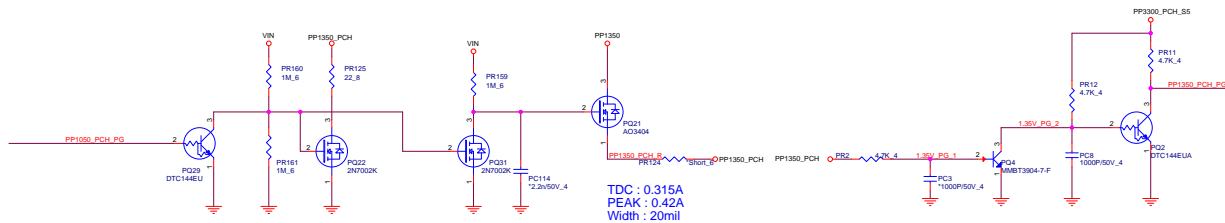
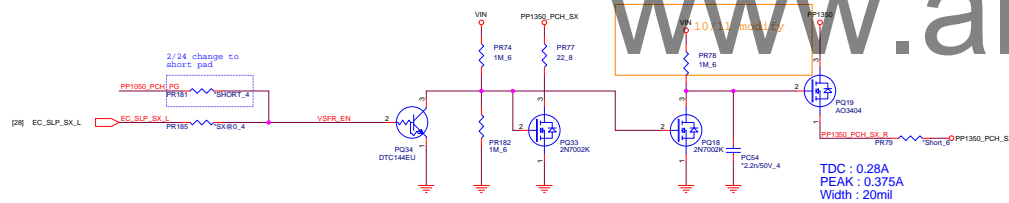
PROJECT :

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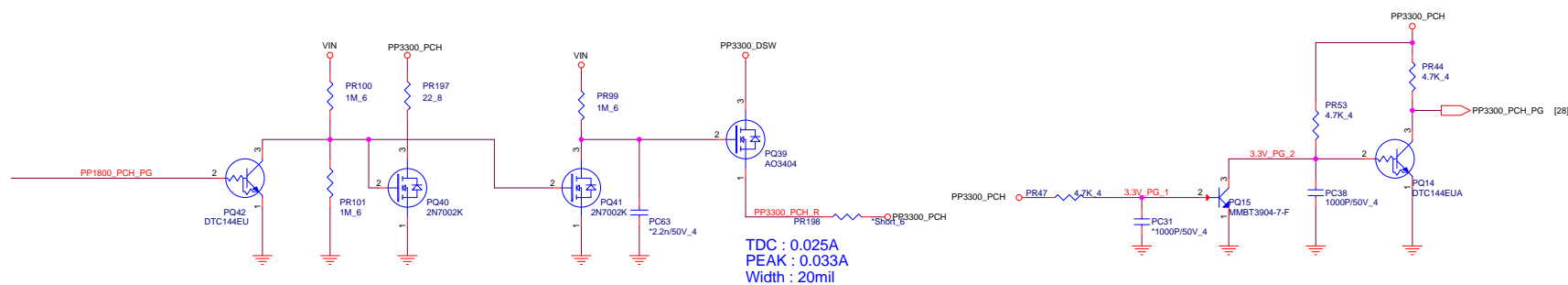
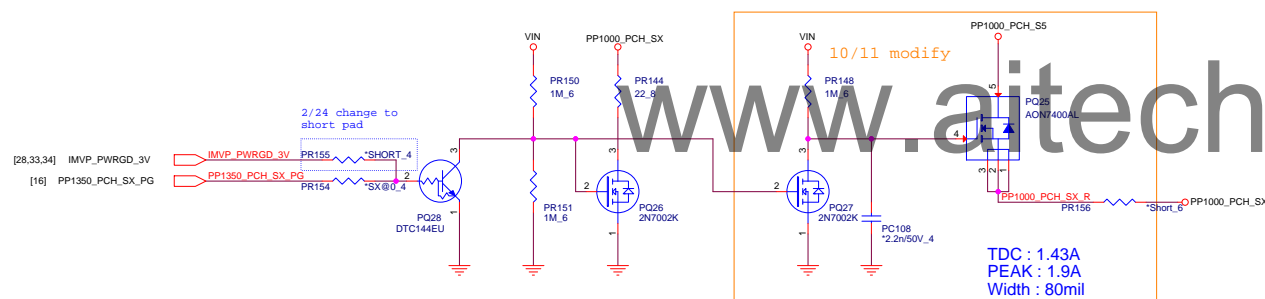
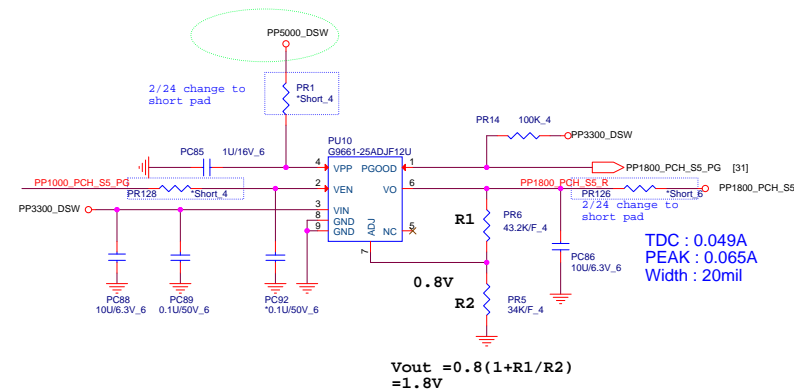








[35] PP1800\_PCH\_PG  
[33] PP1000\_PCH\_S5\_PG





## Thermal protection

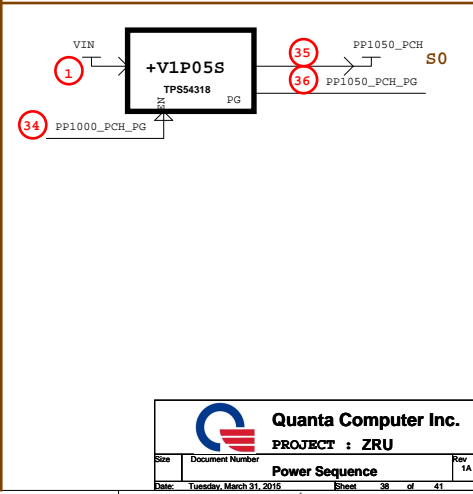
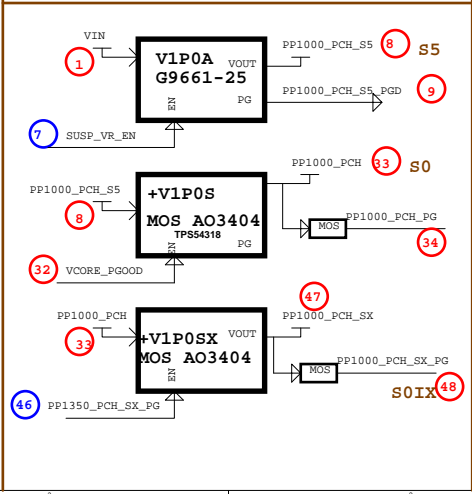
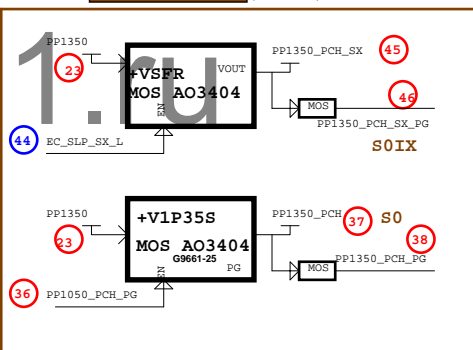
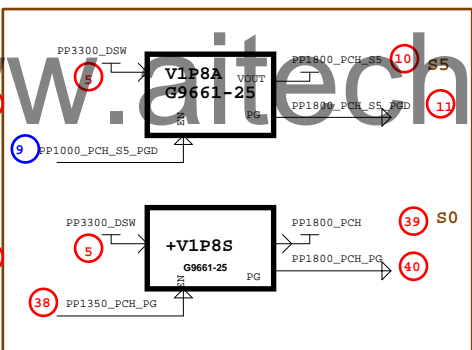
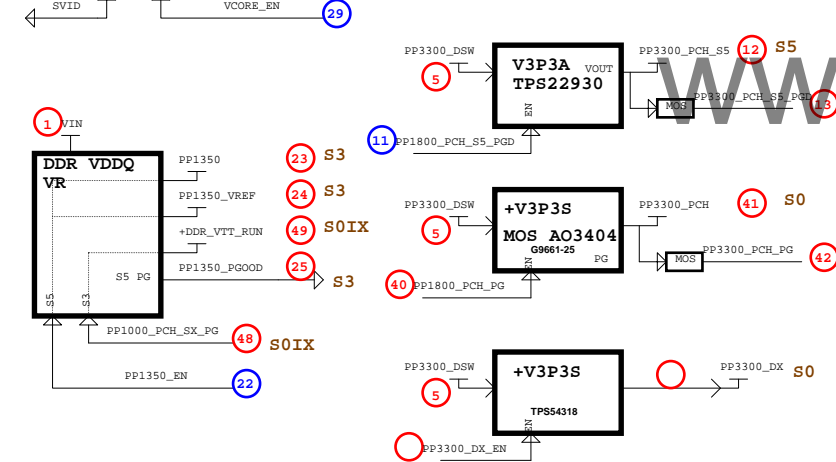
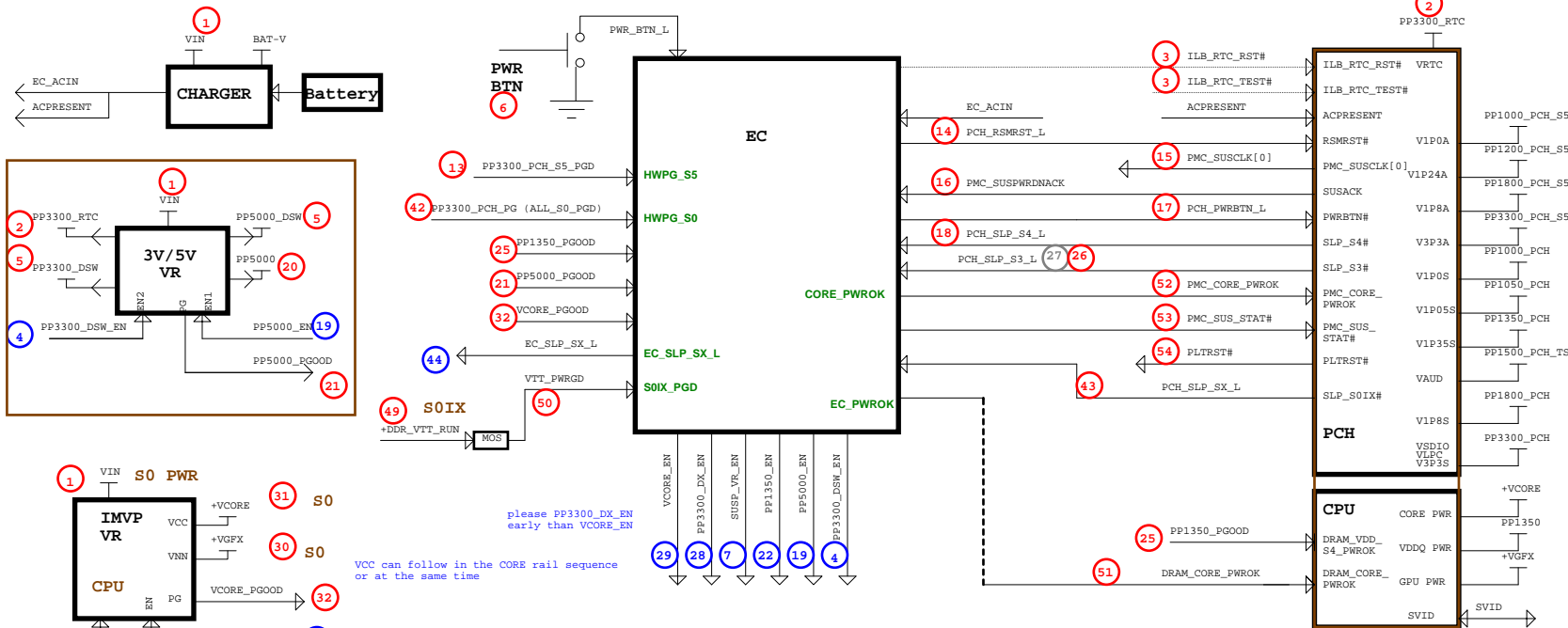
Note placement position



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Rev  
1A

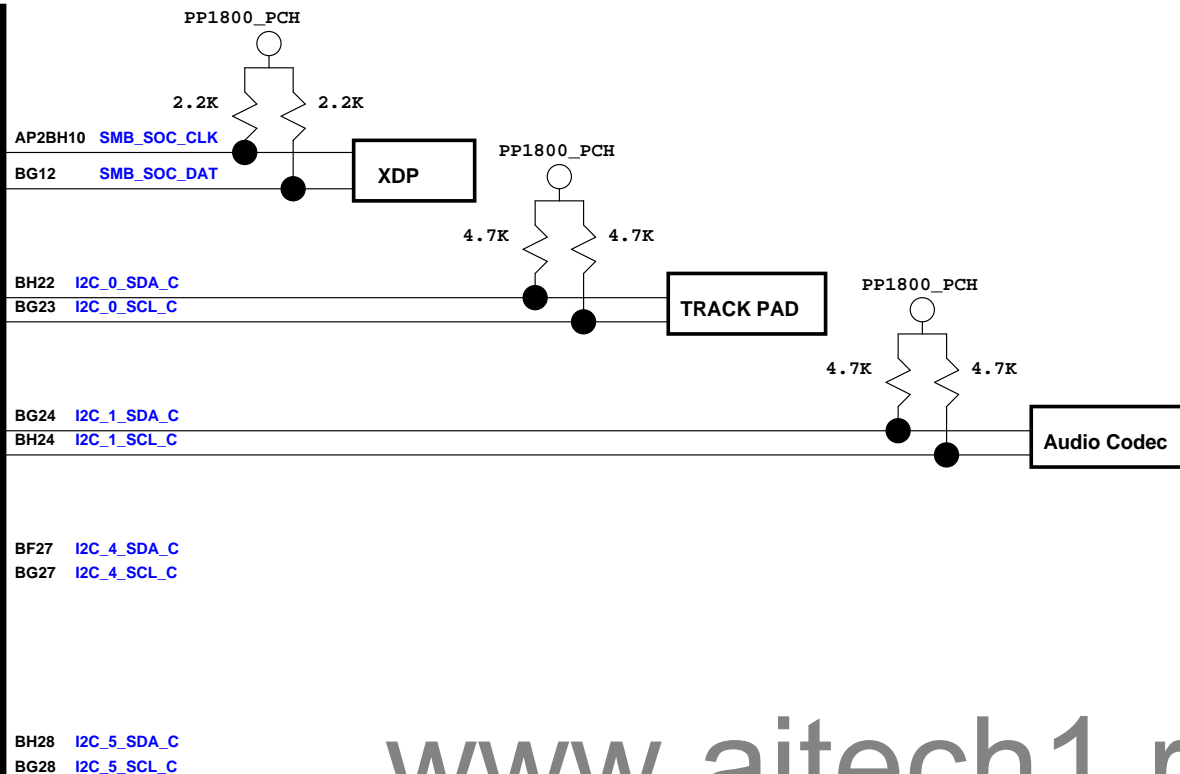
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t1 : RTC\_VCC to ILB\_RTC\_TEST# de-assertion 9ms -min (2-3)  
t1 : RTC\_VCC to PMC\_RSMRST# de-assertion 9ms-min (2-11)  
t2 : V3P3A valid to PMC\_RSMRST# de-assertion 10us -min (8-11)  
t3 : PMC\_RSMRST# to Internal RTC clock stable 100ms -max (11- RTC clock)  
t4 : Internal RTC clock stable to PMC\_SUSCLK[0] toggling 5ms -min (RTC clock - 12)  
t5 : PMC\_SLP\_S4# de-assertion to PMC\_SLP\_S3# de-assertion 30us -min (15-25)  
t6a : Core Well stable to DRAM\_CORE\_PWROK and PMC\_CORE\_PWROK assertion (no PCIe device) 10ms -min (43-45)  
t6b : Core Well stable to DRAM\_CORE\_PWROK and PMC\_CORE\_PWROK assertion (for power rails needed by pcie device) 99ms -min (43-45)  
t7 : DRAM/PMC\_CORE\_PWROK to PMC\_SUS\_STAT# lms -min (45-46)  
t8 : PMC\_SUS\_STAT# de-assertion to PMC\_PLTRST# de-assertion 60us -min (46-47)  
a 10us to 2000us delay is required between rails to avoid inrush current caused by multiple loads turning on simultaneously and fast charging of VR output decoupling

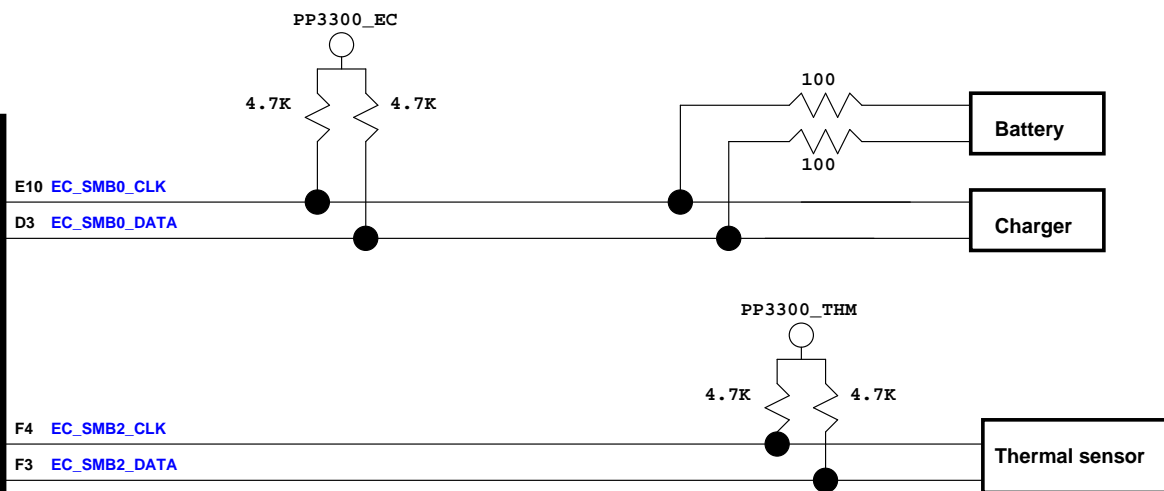
SMBUS  
Bay-trail M

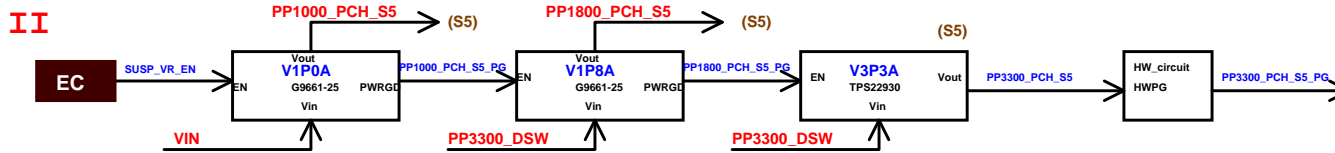
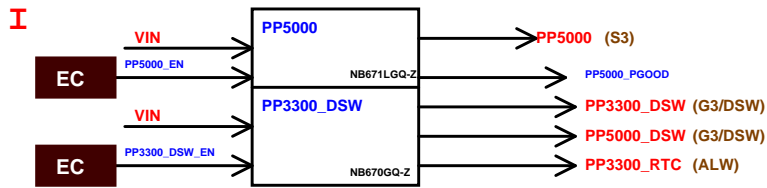
I2C



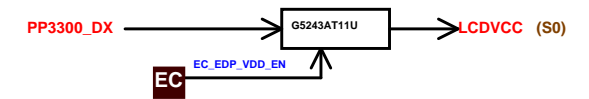
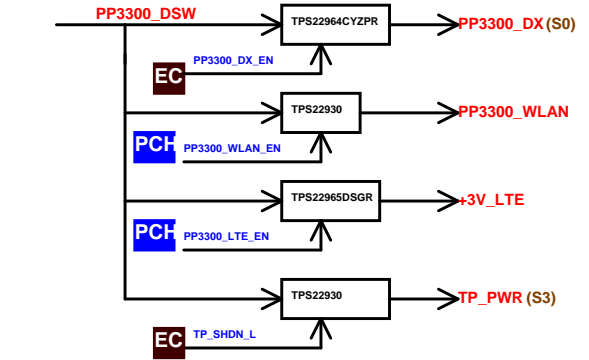
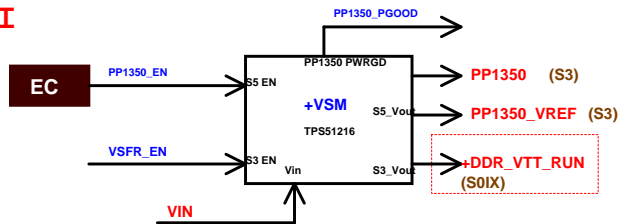
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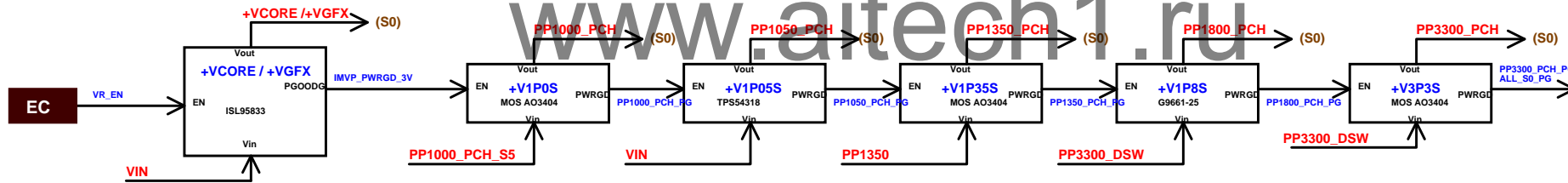




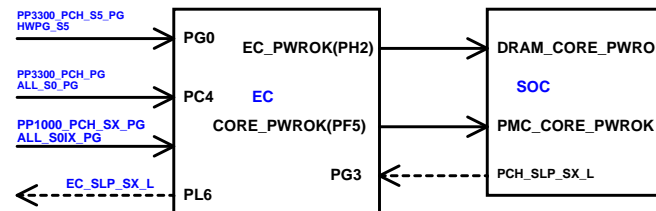
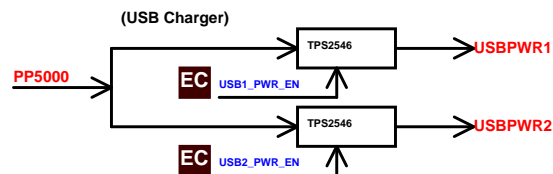
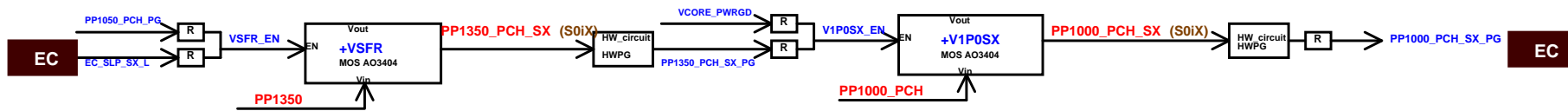
**III**



**IV**



**V**



Model		Version	CHANGE LIST		41
		1A			
	3A	150224: Add USB2PWR on CN12.5 and add GND on CN12.4--page23 150224: Stuff R147,R419,R424,R414 for EMI--page19 150224: Change R97,R90 to short pad--page17 150224: Change R181 to short pad--page20 150224: Change R141,R155 to short pad--page21 150224: Change C283 to 1000pF and Add C357 for EMI--page19 150224: Change L4 to short pad--page27 150224: Remove L14 and change R496,R488 to short pad--page23 150224: Remove L6 and change R430,R431 to short pad--page17 150224: Remove L9,L7 and change R466,R464,R463,R459 to short pad--page26 150225: Change PR1,PR3,PR19,PR20,PR24,PR29,PR30,PR31,PR35,PR40,PR51,PR54,PR59,PR61,PR62,PR65,PR81,PR93,PR95,PR98,PR109,PR115,PR116,PR118,PR122,PR125,PR138,PR146,PR169,PR186,PR189,PR193,PR199,PR200,PR201,PR212,PR155,PR181 to short pad 150225: Change PR8,PR18,PR27,PR33,PR48,PR55,PR73,PR76,PR79,PR80,PR85,PR110,PR111,PR124,PR126,PR153,PR156,PR171,PR188,PR196,PR198,PR213,PR224 to short pad 150225: Change PR92 to short pad 150225: Change JP1,JP2,JP3,JP4,JP5,JP6,JP7,JP8,JP9,JP10,JP11,JP12 to short pad 150225: Uo-Staff PU1,PC3,PC14,PU17,PU20 150225: Uo-Staff PC5,PC7,PC12,PC14,PC139,PC141,PC153,PC160,PC195,PC197 150225: Remove R496,R488--page23 150226: Change PC112,PC126 to CH61001ME96--page34 150226: Update HOLE9,HOLE10,HOLE7 footprint--page26			
	3A	150310: Chnage R119 to 100hm by ESD --page17 150310: Chnage R293 to 330hm by ESD--page27 150310: Chnage C17,C43,C87,C93,C96,C97,C98,C99,C101 to 4.7uF--page10 150324: Add Hole12 by ME add ESD pad--page26 150324:Change D18,D19,D20,D21,D22,D23 to P/N BCPJSD05Z06 by ESD issue. --page26			

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